Version 1, November 2011 **L3X2**

Systems architectures for the LEO III computer.

LEO III is a microprogrammed, transistorised, computer with a parallel arithmetic unit. The architecture is a radical development of LEO II, but with a similar emphasis on efficient data-processing for commercial and business applications. Enhancements to LEO III continued over several years, later (faster) variants being called LEO 360 and LEO 325 – (see below).

The physical word-length of LEO III is 44 bits plus 4 tag bits, though the programmer sees data as either 40-bit long words or 20-bit short words (?). For internal character representation, the 40 bits are divided into five pairs of 4-digit groups, giving five alpha-numeric characters per 40-bit word. The four-bit tag, associated with every long word, is an optional extra. The tag defines the program-number authorised to access that word. If a tag is not matched upon access, an interrupt occurs and the Master Routine deals with the violation.

LEO III has an interrupt facility, enabling several independent programs to be in progress simultaneously. (This was called *timesharing* in the original 1962 literature published by Leo Computers Ltd.; the modern term *multiprogramming* is now more appropriate).

In LEO III the I/O buffers, previously separate, have now been incorporated into the main store. The automatic and independent functioning of the I/O channels has, however, been retained. LEO III has eight concurrent data-communication channels connected to the main store. In LEO III, variable-sized block-transfers to/from peripheral devises are catered for, since the I/O buffers are located in main store.

LEO III has 12 modifier registers, in four groups of three. In addition, any storage location may be used to for indirect modification. The instruction length is (?) 21 bits. As for LEO II, LEO III divides the instruction set into two classes: *address-modifiable* and *address-unmodifiable* (eg shifting and register-to-register ops). Two bit are used either to specify the modifier register *(for address-modifiable* instructions) or to vary (eg extend) the function itself.

The main memory consists of between one and four 4K-word modules of ferrite core store, with early models having a cycle time 13.5 microseconds. Later on, LEO 360's store had a cycle time of 6.0 6 microseconds and LEO 326 had a cycle time of 2.5 microseconds. A store-access control unit handles all traffic to/from the main memory, according to priority. Up to eight input or output channels can be connected to one store access control unit, in addition to the main CPU and a monitor display. Priority is determined by manually plugging devices into particular sockets. Each I/O channel can handle up to eight peripheral devices. LEO III has parity checking on all data transfers.

Arithmetic may be carried out in 'any' radix, thus allowing calculations to be performed on decimal quantities, sterling, weights-and-measures, etc. Fixed-point, floating-point and double-length binary arithmetic is provided. In LEO III, negative numbers are held in sign-and-magnitude form in memory and are automatically converted to 2's complement

representation during arithmetical operations. Also, instructions for sorting, and for compressing/decompressing alpha-numeric information upon input or output are provided.

Here are some examples of peripheral equipment available for LEO III in 1962.

Paper tape reader:	1,000 chars/sec., 5-, 7- or 8-track,
Card reader:	600 cards/minute,
Lineprinter:	1,000 lines/minute, up to 160 chars/line,
Magnetic tape:	Ampex TM2 or TM4 (giving effective data-transfer rates: 18K – 64K chars/sec., at 1,000 char/block).

An idea of LEO III's processing speed (early models) may be had from the following instruction times.

Logical test instruction (average time):	26 microseconds
Addition without modification:	34 microseconds
Addition with modification:	49 microseconds
Multiplication:	226 – 544 microseconds.

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