Version 1, November 2011 **L2X2**

Systems architectures for the LEO II computer.

LEO II was very much like LEO I in respect of its general architecture, though the concept of multiple I/O channels was further developed. LEO II used mercury delay lines but the lines were physically shorter and the access-time was faster than for LEO I. This was because LEO II used pulses of 0.25 microseconds instead of 1 microsecond.

LEO II was basically vacuum tube technology. Later models had large transistorised core stores – (some as large as 8K long (39-bit) words. Supplementary magnetic drum storage was also available for some LEO II machines, transfers being made in blocks of 16 words.

Whereas in LEO I there were four half-adders, two of which were used for accumulator arithmetic, in LEO II all central registers (including the accumulator) shared a total of three full adders/subtractors. One consequence was that multiplication became faster.

LEO II had 19-bit instructions and three modifier registers. The instruction set was divided into two classes: *address-modifiable* and *address-unmodifiable* (eg shifting and register-to-register ops). Two bit in the instruction were used either to specify the modifier register *(for address-modifiable* instructions) or to vary (eg extend) the function itself. The enhanced instruction set included a special counting and testing instruction, whereby a modifier register was augmented and a test made on the count. LEO II also had instructions allowing arithmetic to be performed directly between the 16 ALU registers, and for block transfers to/from drum and to/from magnetic tape.