Version 1, November 2011 **L1X2**

Systems architectures for the LEO I computer.

LEO's central processor was a direct development of the Cambridge University EDSAC. As John Pinkerton, LEO's principal engineer, said: *"The philosophy we had was that we would not change any part of the EDSAC design if we didn't understand why it was done the way it was. So, to start with, since we didn't understand very well why it was done the way it was, we didn't make very many changes at all".*

However, it soon became clear that EDSAC unmodified would not be capable of performing tasks such as the Lyons payroll, which required 18,000 employees' records to be processed in 16 hours or less.

In brief, LEO I had an extended instruction set, more primary memory and comprehensive facilities for bulk data input and output. Whereas EDSAC had mercury delay-line storage for 512 short words – later extended to 1024 short words – from the beginning LEO I had 2048 short words of delay-line storage. Whereas input/output to EDSAC was via relatively slow teleprinter, based on 5-track paper tape, LEO I had independently buffered input and output channels linked to punched card and paper tape readers for input and to punched card punches and line printers for output. Whereas the EDSAC computer contained a total of about 3,000 vacuum tubes, LEO I contained nearly 7,000 vacuum tubes.

Below we first give a description of EDSAC as it was in 1949 and then go on to describe the main enhancements contained in LEO I.

EDSAC in 1949.

EDSAC was a single-address instruction format serial binary computer, with a two-stage *fetch-execute* sequence for each instruction. From the programmers' view, information was handled either as 17-bit short words or 35-bit long words. Instructions were 17 bits long. Negative numbers were represented in the two's complement notation. From the engineers' viewpoint, a long word actually occupied 36 bits, starting with a blank digit-position used as a separator. The same 36 bits could also be treated as two short words, again starting with a blank digit-position but also having a blank separator between the two 17-bit quantities.

EDSAC's main store and the principal central registers were implemented as mercury delay lines (also called *tanks*). The main central registers were:

- Program counter (called the *sequence control tank*);
- Instruction register (called the *order tank*);
- Double-length accumulator (sufficient to contain the result of multiplying two long numbers);
- Multiplier register.

There was no modifier register.

The Arithmetic and Logic Unit (ALU) included a hardware multiplier. The complete EDSAC instruction set is given in section L1X3. EDSAC also had a section called the *Order Interpreter,* which contained the control logic including the function-bits (op code) decoder and the address-selection logic. In the early Cambridge papers, EDSAC was described in block-diagram form, of which the following figure is a simplified version.

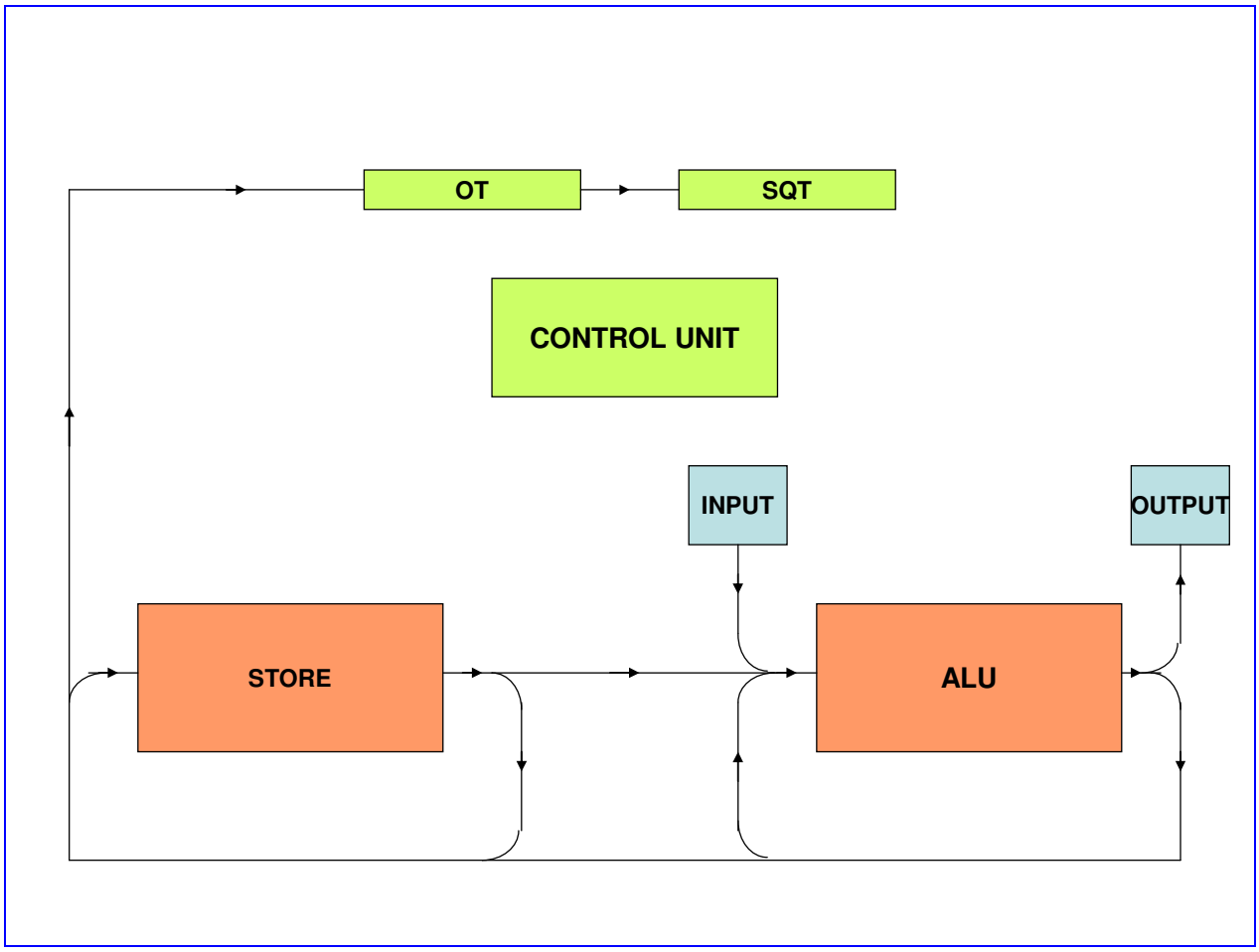

Figure 1: simplified block diagram of EDSAC, showing the main information paths.
OT = Order Tank (the Instruction Register); SQT = Sequence Control Tank (the Program Counter)

Figure 1, which is a reduced form of an original diagram in [**], highlights the circulatory nature of information flow in serial delay lines. The EDSAC main store consisted of a battery of 16 mercury delay lines, or tubes, each one holding 32 short words. All the tubes were kept in a thermostatically controlled 'coffin' to keep the temperature stable. Each tube

EDSAC contained four half-adders: one for the Program Counter (sequence control), one for counting the successive locations circulating in the delay lines of the main store, and two for accumulator arithmetic operations.

Input and output was via 5-track paper tape, as used with teleprinter equipment.

The layout of a 17-bit EDSAC instruction in 1949 was as shown on the next page.

5 bits		*1*	*10 bits*		*1*
Op code		***U***	***Address***		***D***
16	12	11	10	1	0
Most-sig.					*least-sig.*

Op code: a five-bit function code.
U: a spare (unused) bit.
Address: ten bits normally used for a memory address.
D: one bit to signify whether the instruction operated on a short (17-bit) or long (35-bit) number.

LEO I.
The main end-user difference between EDSAC and LEO I lay in the enhanced provision for large volumes of input and output. Figure 2 shows the input/output arrangements for LEO.

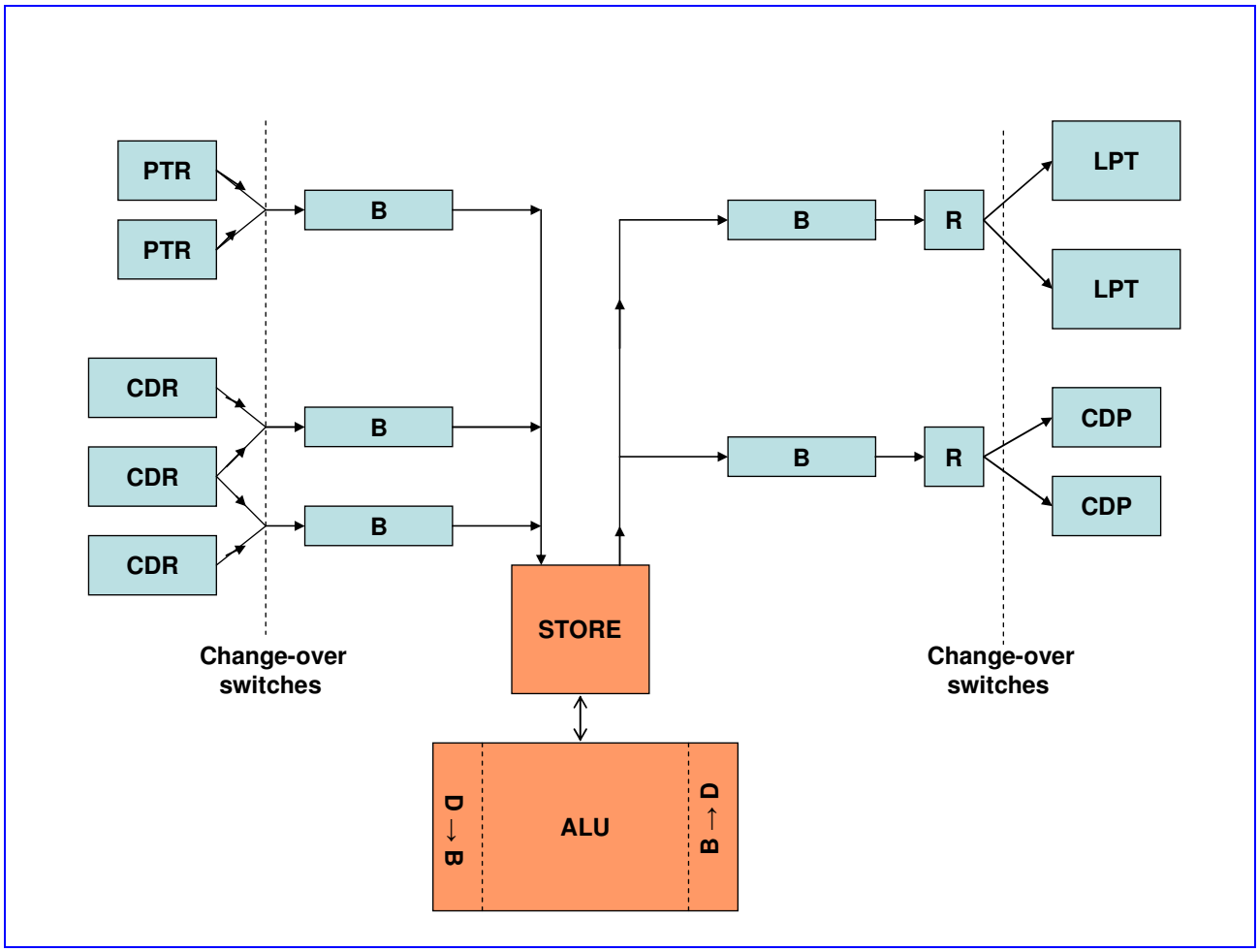

Figure 2: The three input and two output channels for LEO I.

The abbreviations in Figure 2 are explained on the next page.

PTR = 5-tack Ferranti paper tape reader, operating at 200 characters/second.

CDR = BTM card reader, operating at 200 cards/minute (equivalent to about 400 chars/sec.) and using the non-standard scheme of 12 rows of 35-bit numbers.
LPT = lineprinter, operating at100 lines/minute, printing 70 characters/line.
CDP = BTM card punch.
B = 16-word delay line buffer store
R = one-word flip flop register.
D → B = decimal-to-binary conversion hardware
B → B = binary-to-decimal conversion hardware.

Figure 2 shows the 1954 configuration for LEO. The original (1949) plan for input/output was based on banks of input teleprinters feeding data onto ¼-inch magnetic tape decks using the endless-loop system., from whence the data would be transferred at higher speeds into the main computer. The reverse process happened for output, data being fed at higher speed onto magnetic tape decks for subsequent slower off-line printing via teleprinters. This magnetic tape system was sub-contracted by Lyons in 1949 to Standard Telephones & Cables Ltd. (STC), for an estimated cost of £16,000 including circuits for decimal/binary/decimal conversion. In the event, the magnetic tape system proved unworkable and Lyons developed its own system as shown in Figure 2.

The buffered channel system of Figure 2 gave the opportunity for programmers to overlap the essentially faster computing activity with the relatively slower input/output activity. This was crucial in the Lyons' payroll application, where most of the staff were weekly-paid. The calculations per employee had previously taken an experienced clerk eight minutes to perform manually; LEO eventually achieved a time of 1.5 seconds per employee.

As for the LEO central processor, the logic was very similar to that of EDSAC. A two-stage fetch-execute sequence was used, with 1 microsecond pulses at a repetition rate of 514 kHz. However, whereas EDSAC made wide use of EF50 pentodes, LEO re-designed many of the internal circuits to use SP61 pentodes and ECC33 double triodes for reasons of cost-performance.

Mechanically, LEO 1 had 228 sub-chassis, each holding up to 28 vacuum tubes. 12 sub-chassis are mounted in one 9-feet high rack. There are 19 racks. The total power consumption of LEO I was about 30 kW.

The instruction set for LEO I was very similar to EDSAC, except that LEO I included the following extra instructions – (for the complete list, see section L1X3):

Convert, ie decimal-to-binary conversion;
Reconvert, ie binary-to-decimal conversion;
Block input;
Block output.

The extra logic for the Convert/Reconvert instructions used matrices of germanium diodes to store the constants needed (10, 100, 1000 etc.) and a modified versions of the original EDSAC multiplication sequence.

Internally, LEO programmers used 4-bit characters, packed 8 to a word, for alphanumeric data.