The ICT/ICL 1900 Range

"I must say we must have been very brave in those far off days without realising the full implications".
A.C.L. Humphreys CBE (June 1996)

Performance and Competitive position

2-ICT/ICL 1900 Performance and Competitive Position

The assessment and measurement of processor performance became increasingly important with the advent of compatible ranges addressing a large and continuous span of the market. During the 10 years of market life of the 1900 Range, the specification and measurement of processor performance, initially expressed in individual instruction times, was increasingly specified by standardised “work loads”, instruction mixes that could be coded and measured on all models in the range and on competing systems (with different order code formats) .

2.1- Performance of FP6000-Instruction times

The following table details the individual instruction times (and variance) of the initial FP6000:

FP6000 INSTRUCTION EXECUTION TIMES - MICROSECONDS

Configuration →	Standard			With Fast External Accumulators		
Core Store Cycle Time →	2 Usec	4 Usec	6 Usec	2 Usec	4 Usec	6 Usec
Group 0	7	13	18	6	10	14
Group 1	7	13	18	6	10	13
Group 2 except F023	7	13	18	6	10	14
F023	3	5	7	3	5	7
Group 3	7	13	18	6	10	14
F040 - 041	40	54	67	37	45	52
F042	41	57	72	37	45	52
F043	27	43	58	23	31	38
F047	27	43	57	23	31	37
F044 - 046 minimum	41	56	68	38	47	58
maximum	49	65	80	45	53	65
typical	43	57	70	40	48	60
Group 5	5	9	13	4	6	8
Group 6	5	9	13	4	7	8
F070	8	12	15	7	10	11
F072	4	8	12	3	5	7
F074	3	5	7	3	5	7
Group 10	5	9	12	4	6	8
F110, 112	6 + N	12 + N	18 + N	4 + N	6 + N	8 + N
F111, 113	14 + N	28 + N	42 + N	10 + N	16 + N	22 + N
F114	14 + N	26 + N	38 + N	11 + N	17 + N	23 + N
F115	15 + N	29 + N	43 + N	11 + N	17 + N	23 + N
F120 - 122	5	9	12	4	6	8
F123	3	5	7	3	5	7
F124	6	10	14	5	7	9
F125	4	6	8	4	6	8
F126	13 + 4N	23 + 8N	32 + 12N	11 + 4N	17 + 8N	22 + 12N
F127	14 + 3N	25 + 5N	32 + 7N	12 + 3N	19 + 5N	23 + 7N
To index an instruction add to above	2	4	6	1	1	1
Floating Point with X	34	48	62	30	36	42
External +	64	78	92	60	66	72
Floating Point +	24	38	52	20	26	32
Unit -	24	38	52	20	26	32

2.2- Performance of ICT 1900 in 1966

This table, extracted from an ICT document (November 1966), gives to prospective customers some key figures for each member of the ICT 1900 Range.
Performance figures are the major part of its contents.

The performance of small scientific loops is included in the table. An assessment of the relative power of each relevant model of the range in the execution of this type of work is also included.

I.C.T. 1900 Series (in 1966)
Characteristics of central processors

		1901	1902	1903	1904	1905	1906	1907
Core store cycle time (micro-seconds)		6	6	1.8 or 2	2	2	1.1 or 2.1 up to 1.25 or 2.25 for largest core store	1.1 or 2.1 up to 1.25 or 2.25
Data channels (maxima)	general	3/6	8	8	18	18	18	18
	fast	—	—	—	5	5	any number	as required

		1901	1902	1903	1904	1905	1906	1907
Arithmetic times:							(At 1.25 µS cycle time)	
Fixed point	add/subtract	34 µS	18 µS	7 µS	7 µS	7 µS	2.5 µs	2.5 µS
	multiply	4.7 ms	1.5ms	650 µS	40 µS	40 µS	10.05 µS	10.05 µS
	divide	7 ms	2.3 ms	900 µS	44 µS	44 µS	18 µS	18 µS
	jump	21 µS	13 µS	5 µS	5 µS	5 µS	2.5 µS	2.5 µS

		1901	1902	1903	1904	1905	1906	1907
Floating point	add/subtract	Floating point arithmetic is available				13 µS	185 µS	4 to 7.25 µS‡
	load					6 µS	115 µS	0.5 to 2.5 µS‡
	store					8 µS	110 µS	1.25 to 2.5 µS
	multiply					29 µS	290 µS	10 to 13.25µS‡
Address modification†						2 µS	625 µS	0.625 µS
Scalar product loop x' = x + a;b;						60 µS	700 µS	24.2 µS
Polynomial loop x' = x (x + a;)						42 µS	480 µS	16 µS
Approximate agreed ratio for performing typical scientific calculations based on the above polynomial loop			1	2-5	11	250	22	650
Number of time-shared programs		1	1	1	4	4	16	16
each with sub-programs			2	2	2	2	3	3

Word length:
Fixed point: 24 binary digits—four alpha-numeric characters.
Floating point: Argument 37 bits plus sign. Exponent 8 bits plus sign.

†1905 and 1907 processors incorporate floating point unit. Address modification of most floating point instructions takes no extra time due to overlapping of instructions.

‡According to context

This specification is subject to modification

2-3 Performance of ICT / ICL 1900 Series (All Models) and derivatives 2903/ME29

In a compatible range, addressing a wide and continuous span of the market, it became increasingly important to position each model in the range relative to the other models.
Careful spacing of processors performance in the range ensured coverage of the market span with the minimum of models, without leaving significant gaps, with the resulting savings in development costs, production and sales costs.
The need to specify and measure processor performance in a more meaningful way led to the definition of "Work mixes", representative loops of instruction that could be coded and run meaningfully on all machines.
Amongst the most widely used mixes were POWU2, GAMM, Gibson, Knuth (Fortran) and Wichmann (Algol).

ICT used extensively POWU2 as a performance measurement of "commercial" data processing (without Floating Point instructions) and GAMM mix for "scientific" computing (dominated by Floating Point instructions).
POWU2 was of particular importance. Specified by the UK Post Office (**P**ost **O**ffice **W**ork **U**nit2), it was used to specify performance in UK government purchases.

In ICT (and later ICL) it was used in the specification of product requirements, in the measurement of the performance of competitive systems and in the setting of system prices in the market (in general, 1900 prices were set at 5% below the IBM360 (later IBM370) price performance curve).

The following is an extract from an ICL document on performance (dated 1972):

> "e) On some machines it is possible to code the POWU 2 in various ways, each producing different results. The figures quoted for such machines are not necessarily the optimum obtainable within the POWU 2 definition but are intended to be realistic in terms of actual processing.
>
> f) The instruction sets of different ranges of machines (within ICL and competition) are not identical and the number of instructions required to code POWU 2 accordingly varies from one machine to another. On 1900 there are 880 instructions in the loop.
>
> g) For multi-processor configurations each processor can be rated separately but no general statement can be made to represent the power of a total system without reference to specific workloads.
>
> Some manufacturers quote the instruction processing rate of their CPUs. In some cases, however, this is the rate of processing the shortest instructions and not the average of a typical instruction mix."

Original 1900 Series

The following table was measured in term of POWU 2 and GAMM after first deliveries and it is included for completeness.

System	First Delivery	Performance			Clock nS
		POWU 2 ms.	POWU 2/Sec	GAMM uS	
1907 (1Us)	1967	4	268	12	750
1906 1us	1967	4	268		750
1907 (2us)	1967	5	200	14	750
1906 2us	1967	5	200		750
1909	Aug-65	7.5	133	29	
1905	May-65	8	133	29	1000
1904	1965	7.5	133		1000
1903	1965	18	55		1000
1903 EMU		16	64	86	1000
1902	1965	45	22		
1902 EMU *		40	25	116	
1901	Mar-66	83	12		4000
1901 EMU *	1966	67	15	130	4000

**EMU = Extended Mathematical Unit*

The E/F's

The E/F series used the same hardware technology as the original 1900, but included significant optimisation of the design and significant enhancements of the 1900 architecture.
The resulting improvement of the performance should be noticed (a single 1904/5 F almost reaches the performance of the original 1906/7).
The raw computing power available in an anonymous dual processor system (1906/7E/F) was measured at 1.8 times a single.

System	First Delivery	Performance			Clock nS
		POWU 2 ms.	POWU 2/Sec	GAMM uS	
1907 E/F	1968	1.8x1905 E/F			750
1906 E/F	1968	1.8x1904 E/F			750
1905E	1967	6	158	29	750
1905E (H/W Registers)	1967	5	189	28	750
1905F	1967	4.3	233	18	750
1904E	1967	6.3	158		750
1904E (H/W Registers)	1967	5.3	189		750
1904F	1967	4.3	233		750

The 1900 A Series

Having achieved a well understood and stable architecture, ICT applied state of the art integrated circuit technology and the necessary advanced packaging technology, with significant improvements in the competitiveness of the 1900 range.

System	First Delivery	Performance			Clock nS
		POWU 2 ms.	POWU 2/Sec	GAMM uS	
1906A	1970	0.9	1111		100
1904A	1969	3	333	11	500
1903A	1968	5.8	172		720
1903A SCF‡	1968	5.8	172	44	720
1902A	1968	21	47		1500
1902A CCF†/SCF‡	1968	11	87	87	1500
1901A	1969	63	16		
1901A CCF†	1969	45	22	109	

† CCF= Commercial Computing Feature (Group 4 instructions- Fixed Point Multiply/Divide and I/O conversion)
‡SCF= Scientific Computing Feature (Group 13 FP instructions – held FP Accumulator)

The 1900 S series and 1900 T's

The 1900 S series, the last to span the whole range, was mainly an evolutionary enhancement, achieved by selectively applying faster technologies to the 1900A designs. This development achieved very significant performance improvements with relatively modest development resources.

The 1900 T models, introduced in the lower part of the range. were mainly a re-badging (and cost reduction) exercise. Performance and specification improvements for each model were achieved mainly by regrading the higher model.

System	First Delivery	Performance			Clock nS
		POWU 2 ms.	POWU 2/Sec	GAMM uS	
1906S	1973	0.65	1540		100
1904S	1972	2.3	435	10.5	300
1903S	1971	5.8	172	44	640
1903T	1973	4	250	15	
1902S	1971	11	87	87	1500
1902T	1974	7	152	55	1000
1901S		50	20		
1901S CCF†		31	32	90	
1901T	1974	13	76	95	

The 2903 and ME29

The 2903 series, an innovative design still using 1900 order code, was introduced shortly before the announcement of the 2900 mainframes models (hence the name and its "tango" skin).
It was competing well in the "low cost" computing market. Addressed to small companies without a DP department, ease of use was more important than the raw performance of its processor.

System	First Delivery	Performance			Clock nS
		POWU 2 ms.	POWU 2/Sec	GAMM uS	
2903/25	May-76	23	44		540
2903/40	May-74	17	60		540
2904	May-76	9	111		540
ME29	1980	7	150		

2.4 ICT 1900 competitive position

At the end of 1963, when the newly merged ICT was in the early phase of development of the 1900 Range, ICT was the number one supplier in the UK (the UK was probably the only major country in the world where IBM was not the dominant supplier). To maintain credibility and market share, ICT had to market, and to keep competitive, a range of 1900 systems equivalent to the IBM 360 range. But the IBM R&D spend at the time was greater than ICT total revenues.

ICT had a technical interchange agreement with RCA, but, having decided to adopt the 1900 range in preference to the IBM compatible RCA Spectra 70, ICT had to develop, market, manufacture and support the complete range from its own resources.

The competition

Many other computer companies were very active in the period 1964-74, some of them being:

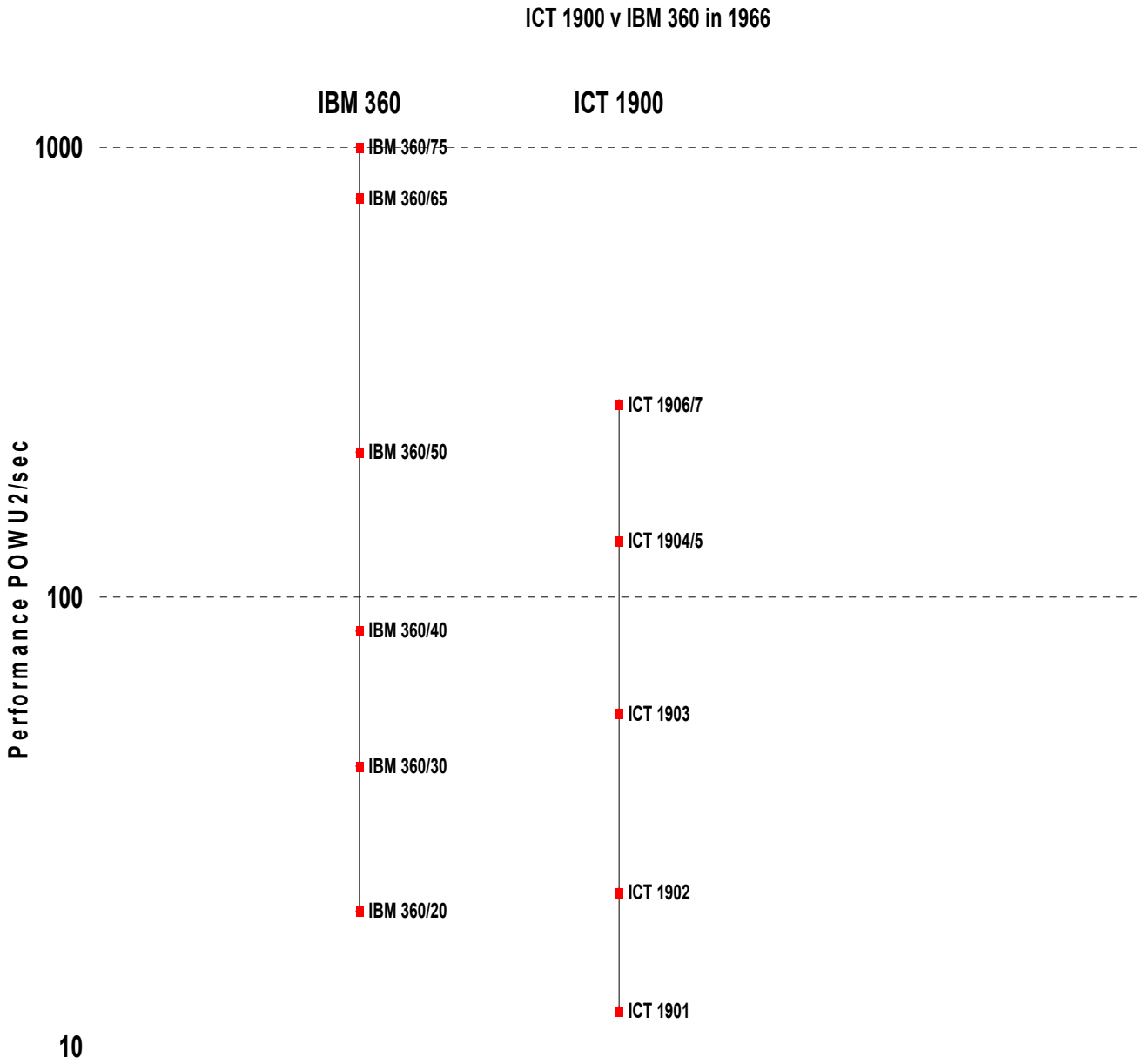
Burroughs (B2500, B3500 etc. and B1700, B2700, B3700, 4700, 6700, 7700)
CDC (6400, 6600 and Cyber 72, 73, 74, 76)
DEC (System10)
Honeywell (2000 Series and 6000 Series)
NCR (Century)
Univac (9000/Series 90 and 1100 Series)
RCA (Spectra 70)
GE (400 and 600 Series)

But, though the above systems were monitored and considered when assessing the competitive scenario, “The Competition” was IBM with the IBM 360 Range and, later, the IBM 370 Range.

From a performance point of view, the 1900 range competed well with the lower part of the IBM 360 range and, with the arrival of the 1901, had a lower entry point.
But at the higher part of the Range, the 1900, given parity of hardware technology, could not compete well with the top members of the IBM range when comparing “commercial” performance in single (i.e. not multiprocessing) systems. The need to be in this area of the market with its emerging advanced applications (i.e. Real time transaction processing), prestigious customers and high profitability, provided impetus towards the early development of (anonymous) multiprocessors systems, and it was one of the factors leading to the introduction of the 2900 range in 1974..

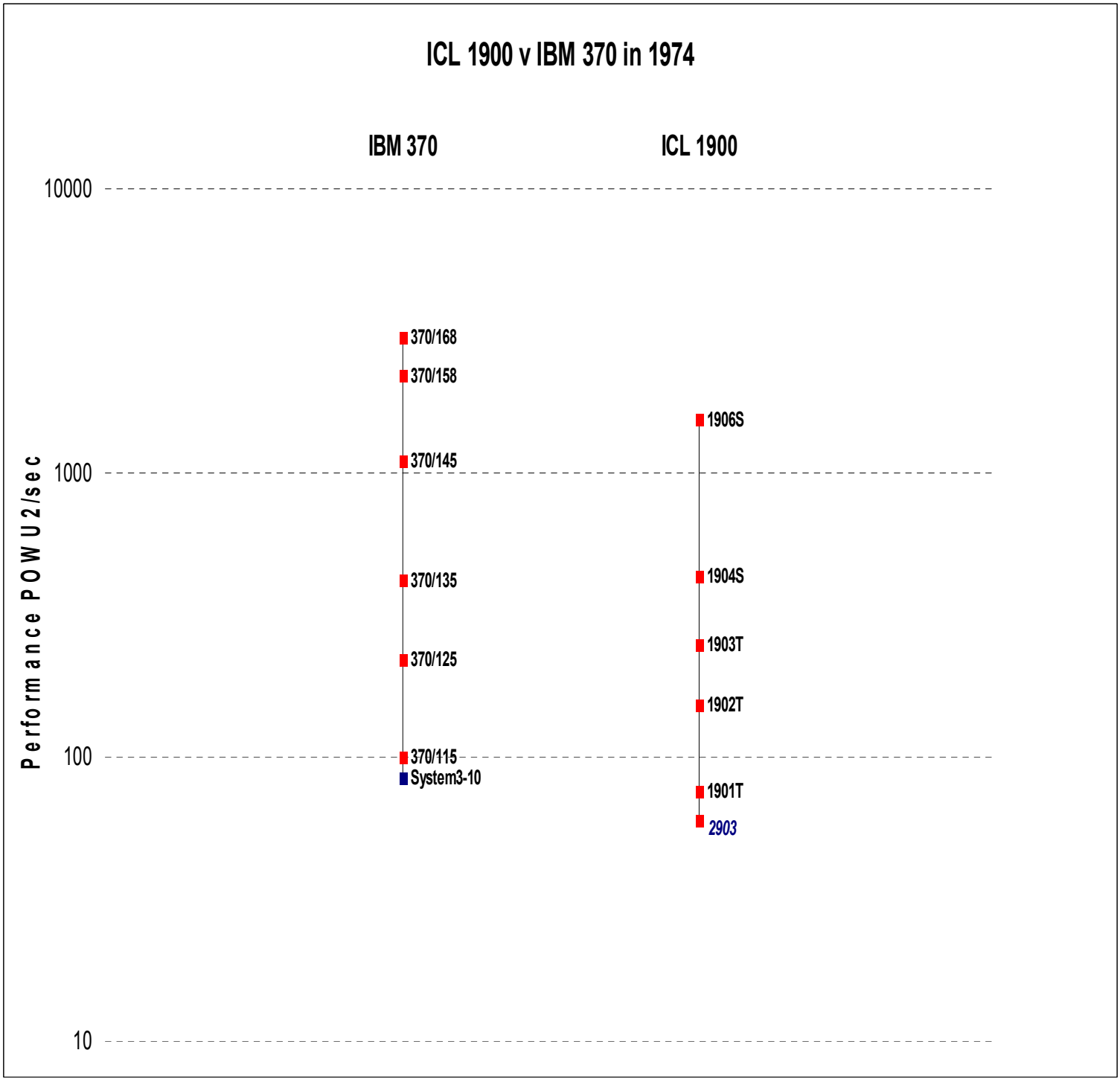
ICT1900 and IBM360 in 1966

By 1966 both the IBM 360 and the ICT 1900 were settling down after an initial period of turmoil. The following diagram plots the IBM 360 range and the ICT 1900 range positions in 1966(in terms of single processor performance measured in POWU 2/Sec)



ICT1900 and IBM370 in 1974

Looking at the competitive position in 1974 in terms of data processing performance, ICL (as it had then become), by the application of very advanced and fast MECL10k technology and the necessary packaging and cooling technology, had improved its relative position at the top of the range.
ICL was delivering a range of competitive 1900 systems (the S and T series) using advanced designs with "state of the art" technology.



Besides maintaining the range competitive, in 1974 ICL had introduced the 2903 (a new 1900 compatible system) below the bottom of the 1900 range, competing with the IBM System 3. ICL development teams were also well advanced in the development of the three top models of the New Range (ICL2900 Range).

Conclusions

The following chart maps the span of the two ranges (ICT/ICL 1900 and IBM 360/370) in 1966, at the beginning, and in 1974, towards the end of the 1900 as a full range.
It shows that, despite great disparity of resources, by 1974 ICL had actually increased the span of its 1900 range, at least in terms of processor performance.
The ICT (and ICL) engineers adopted successfully a “technology intercept” policy by working very closely with IC’s manufactures and other innovative suppliers to take into account technologies under development and adopt them early.