The ICT/ICL 1900 Range

"I must say we must have been very brave in those far off days without realising the full implications".
A.C.L. Humphreys CBE (June 1996)

Architecture and Systems description

1 – 1900 Range – Architecture and Systems description

1.1 - How the ICT 1900 Series evolved.

In 1962, the Canadian Ferranti subsidiary, Ferranti Packard, had quickly designed and produced the FP6000 computer, after a lengthy visit to the UK to study Ferranti UK ideas (including Orion). The first FP6000 was installed and running at the US Federal Reserve Bank in New York in March 1963.

In 1963 the Ferranti Computer Department in the UK had a need for a system in the medium price range, below the performance level of Atlas and Orion, as a successor to the Ferranti Pegasus, Mercury and Sirius systems. This prompted a visit to Toronto in March 1963 by a UK team to study all aspects of the FP6000 to assess its suitability, with modifications if necessary, to meet Ferranti's needs.

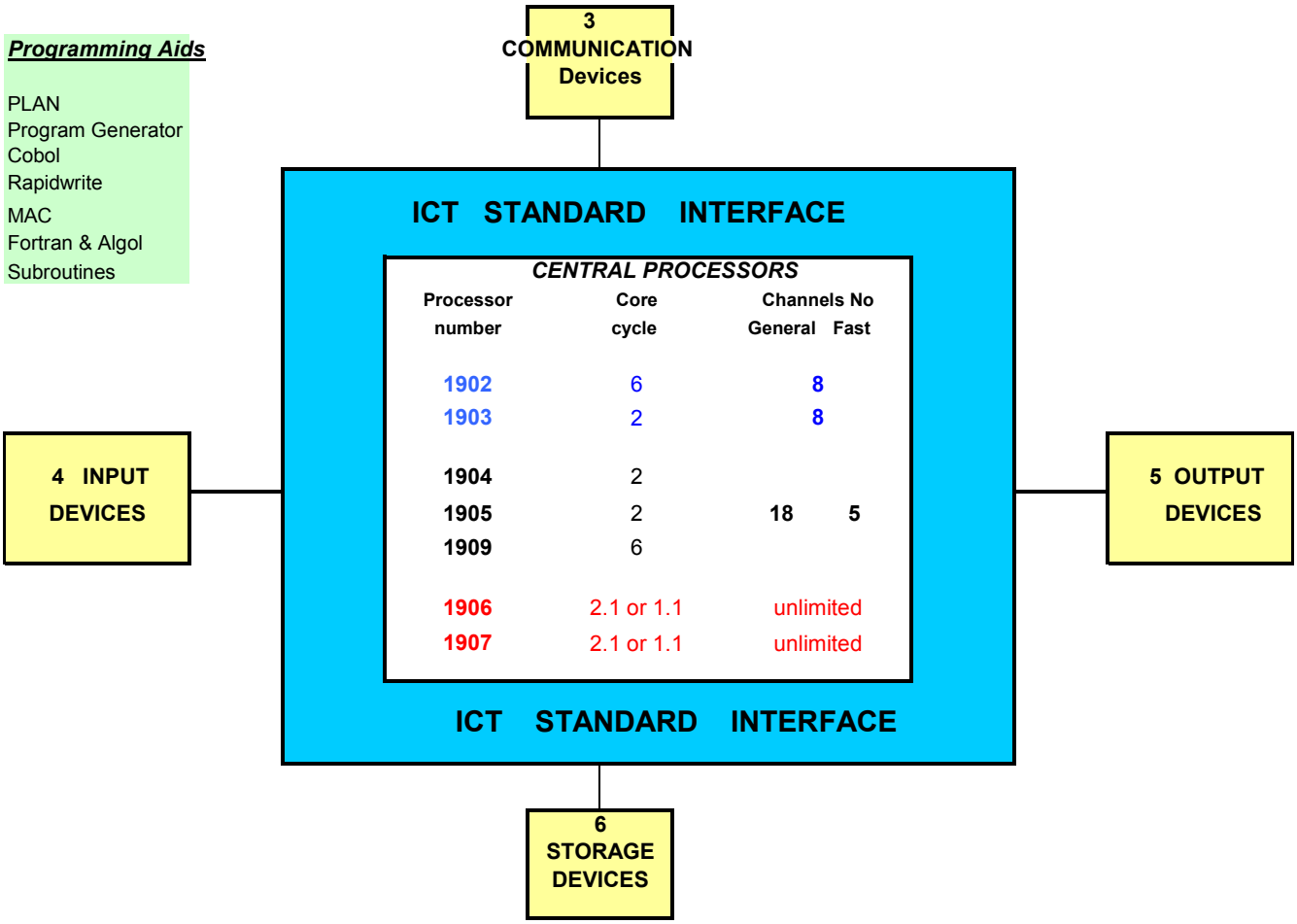
The team concluded that
"There are certain facets of the system we do not like. However, were we to begin designing now a machine in the same price/performance range as the FP6000, we would have in some 18 months' time a system that would not be significantly better - if indeed it were any better - than the FP6000."

It was becoming clear that IBM was planning a compatible range of machines covering a large spread of processing power, and the Ferranti need to be able to deliver proven hardware quickly was probably the key factor in the decision to adopt the FP6000 design as the basis of the new Ferranti range of systems. An FP6000 was delivered to Ferranti West Gorton Labs, another to Ferranti Bracknell, and development work started on the new Ferranti medium system range, the 1900 (that later became the 1904/5).

From January 1963 ICT was exploring with Ferranti a merger of the Ferranti Computer Dept. with ICT. Very soon after the publication of the Ferranti FP6000 visit report a joint ICT/Ferranti party including Arthur Humphreys, "Echo" Organ and Tom Sheppard from ICT and Peter Hall and Hugh Devonald from Ferranti visited New York and Toronto to assess the FP6000. After September 1963, when the ICT shareholders approved the acquisition of the Ferranti Computer Dept. by ICT, development work started in ICT Stevenage on the1902/3, while ICT (Ex Ferranti) West Gorton Labs initiated development of the 1906/7 to complement the already ongoing development of 1904/5 (FP6000), both projects under the overall leadership of Charlie Portman.
Some key architectural changes were introduced to make the FP6000 design better suited to be the basis of a wide compatible range., the key ones being order code changes to allow expansion of memory capacity beyond 128K 6 bit characters (32K 24 bit words), initially in the 1906/7, and the introduction across the range of the ICT Standard Interface that had been specified by the ICT Stevenage Labs and RCA.

Confronted with challenging timescales, the teams of engineers from the development labs of the newly merged company worked together in an extraordinary spirit of cooperation and mutual respect to achieve immediate outstanding results. The ready acceptance of the Ferranti 1900 design by the ICT development engineers (especially the excellent ex-EMI people who formed the nucleus of those assigned to the work at Stevenage) and the ready adoption by the ex-Ferranti engineers of the ICT Standard Interface was, to say the least, unusual for those times.

The ICT engineers in Manchester West Gorton and Stevenage were able to develop 2 working systems (1903 and 1904) to be exhibited at the Business Efficiency Exhibition at Olympia (London) immediately after the ICT 1900 Announcement of 28 September 1964 (some six month after the IBM announcement of the 360). While the timescales achieved by both development teams were short by the standards of the time, particularly noteworthy was the achievement of the Stevenage team, led by Norman Brown under Mike Forrest and Bill Talbot. The team produced in one year a working 1903 without previous knowledge of the architecture.



ICT 1900 Announcement Summary (Simplified extract from ICT document Sept 1964)

ICT announced a range of seven 1900 system models (1902, 1903, 1904, 1905, 1906, 1907, and 1909), Programming Aids (Software) and peripherals.
In the announcement, great emphasis was placed on programming compatibility and portability between all models in the 1900 range (present and future) and modularity via the ICT Standard Interface ("Each 1900 system will grow with the customer's needs by replacing individual modules as needed, without needing to replace the whole system"). Another key message was "value for money". Storage discs (both fixed and exchangeable) were announced, but initially emphasis was placed on Magnetic Tape systems.

The first 1900 system (1905) was delivered to Northampton CAT (City University) in May 1965, in advance of IBM 360 deliveries. Deliveries of the other 1900 systems started during 1965.

A year later the range was extended with a new system, the 1901, of approximately half the power of the 1902. The 1901 was a key addition to the 1900 range. It extended downwards the 1900 range into a price area that IBM normally could not reach with the 360 range. ICT was able to provide entry into its fully compatible range at a price well below the 360 level.

Subsequently, a system below the 1901 and one at the top of the range (the 1908) were investigated and defined, but they never went into full development for different reasons.

With the addition of the 1901, the viable span of the 1900 range was established, and this span continued in the subsequent manifestations of the 1900 range till the ICL top down announcement of the 2900 in 1974.
The 1900 was in continuous development during this period:

The first phase of development after the original 1900s, while keeping the same processor hardware technology, concentrated on improving key aspects of the architecture (see 1.4), and produced the 1904/5 E/F and 1906/7 E/F, replacing the 1904/5/6/7/9. Extended addressing, dual systems and the introduction of Segmentation and Paging as an alternative to Datum and Limit were the major improvements.
The subsequent phases of development, taking advantage of a stable and well understood architecture, applied state of the art technologies to the designs.

- On 17 January 1968 the **1900A series** was announced (1901A, 1902A, 1903A, 1904A, 1906A) replacing the whole range.
- On 29 Jan.1968: 1000th order taken for 1900's
- On 28 April 1971 the **1900S series** was announced (1902S, 1903S, 1904S, and 1906S). Later 1901S
- In 1973 and 1974 the **T models** were introduced (1901T, 1902T, 1903T) in the lower part of the range, while the 2900 Range was under development to replace the upper part of the range. The 2900 started to replace the 1900 top down from 1974.
- In March 1974 the first 2903 was delivered. Though, strictly speaking, not part of the 1900 Range, the highly successful1900 compatible **2903 family** and its successor (**ME29**) continued to sell till the 1980s in the lower part of the market.
- The 1900 software continued to run on the 2900 (in DME and CME* modes)

1.2 - The ICT 1900 Range in 1966

After the introduction of 1901, the first manifestation of the 1900 Range was complete. The following is an extract from an ICT brochure (Nov. '66), describing the full range and emphasizing what, at the time, was considered important and innovative in the ICT 1900.

"**I.C.T.** has designed the 1900 Series from the beginning as a complete series of systems, in which all central processors and peripherals are of one family and all equipment, programs and data representation are compatible. All necessary facilities both for commercial and scientific applications are incorporated. In scope the Series extends from a configuration priced as low as £28,000 to one of £750,000 or more. This is what it offers to every user:

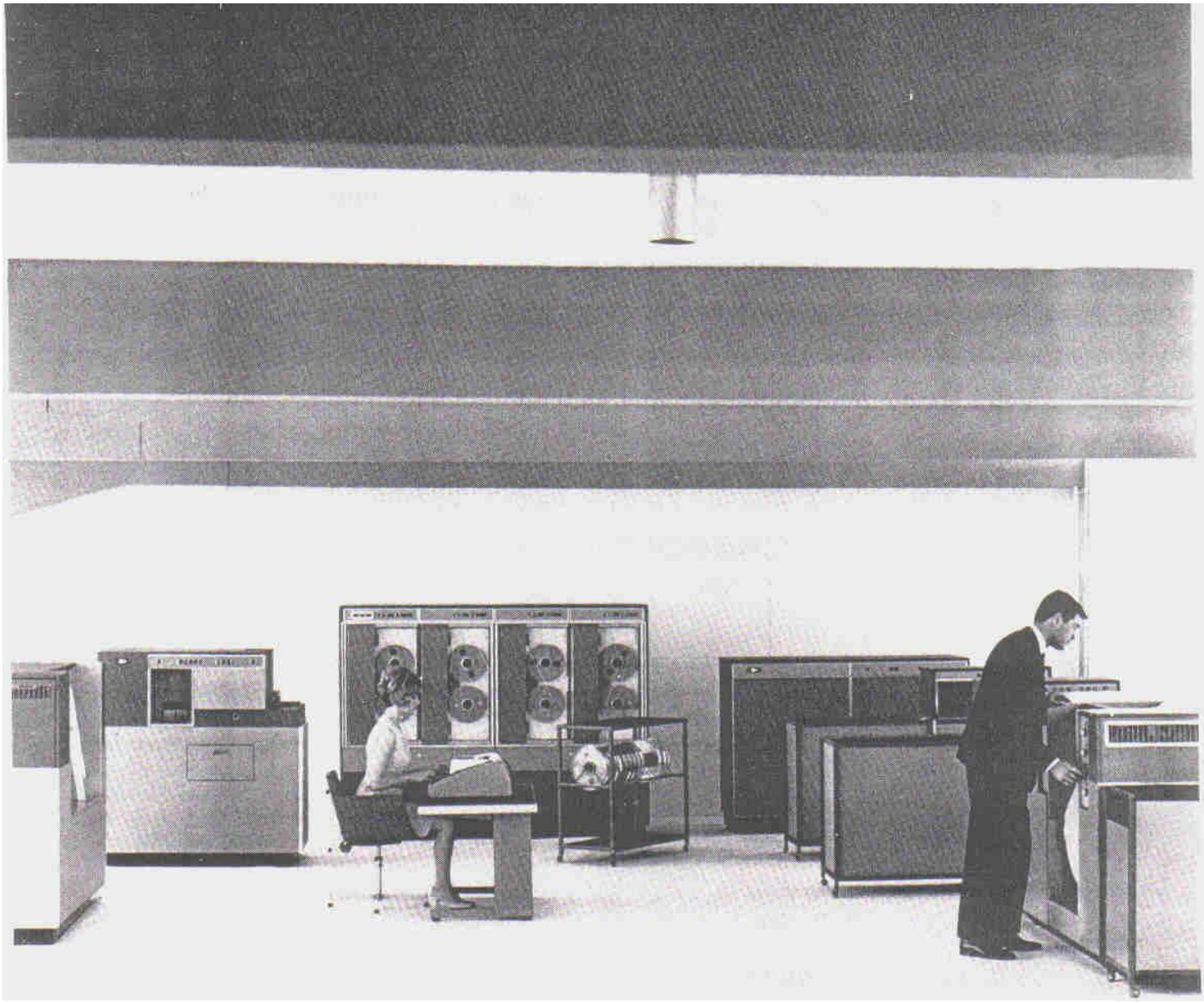
Freedom of Choice The 1900 Series has an extensive range of compatible processors and peripherals, enabling the user to choose the initial configuration best suited both to the volume and to the type of work that he is ready to load onto the system now. He can start economically, without overspending either in terms of manpower or money.

Freedom to Expand The 1900 Series thrives on growth both in volume of work and in scope of operations in any application. It grows with the user as he grows. It provides additional facilities as he needs them. Whether the requirement is on site or far afield, the communications facilities of the equipment permit virtually unlimited expansion. The 1900 Series is designed round the concept of Standard Interface, through which standardized sets of signals transfer information between all processors and all peripheral devices. All components thus become fully interchangeable. Complete flexibility is provided throughout the system, and new peripheral devices can be attached to an existing processor. Conversely, if and when more work capacity is required more core storage can be added or a more powerful central processor can be substituted, the existing peripheral units being retained. Processors communicate with each other and with the peripherals of their own and other systems. Expansion through the linking of a network of individual systems is therefore made possible.

A Single Programming Investment The I.C.T. 1900 Series is simple to program because it has been designed around comprehensive and simple programming languages, which are common to every processor in the series. The original investment in programming is not lost as the user expands his 1900 Series installation, and indeed will not be lost whatever developments take place within the I.C.T. range of computing systems.

Simplicity in Operation Communication with the 1900 Series is simple. A typewriter passes instructions to the computer system in plain language and from there "Executive" —the Master Program—takes over. "Executive" is a special program provided by I.C.T. which supervises the operation of the system for the user. It reports upon the progress of programs and the state of peripheral devices, controls the transfer of information and generally oversees the functions of each component device in the system. It also continuously monitors performance, to ensure accuracy and to avoid any possibility of error.

Vast Variety and Capacity of Storage The I.C.T. 1900 Series provides data storage devices from magnetic drums, through exchangeable disc stores to the largest scale file storage devices, such as the magnetic card file. These provide immediate access at a cost lower than comparable systems. The user can therefore choose from a selection of random access devices in the area of cost appropriate to his work, and open the door to a new approach in management techniques.



Detailed specification

This section shows the full scope of the choice in central processors, input and output peripherals, storage, display devices and communications available now.

Central Processors

All central processors may be specified; all designed to obey the same instruction code so that programs written for the smallest machine can be processed by any in the series. All the processors are expansible on site and can be replaced by a more powerful processor. This is possible because all peripheral devices—input, output, storage and communications—are attached to the processor via I.C.T. Standard Interface.

Instruction Code
The instruction code, common to all machines in the series, is extremely powerful and very comprehensive. Functions which are performed by circuits in the faster processors are called by "Extracodes" in the simpler versions.

Standard Interface
This feature makes it possible to connect peripherals of different functions and speeds to the central processor, handling transfers to and from the peripheral to which it is connected. Devices of the future will also be linked to the processor by this means.

Performance

1901 Processor: The smallest in the range, this processor is designed to provide a new low-cost data processing system that is suitable for the small to medium-sized business. The 1901 has either 4,096, 8,192 or 16,384 words of core store with a cycle time of 6 microseconds. Like all 1900 Series processors, the word length in the store is 24 binary digits. Three standard interface channels are provided with provision for three more. The number of peripheral devices employed can however exceed the number of channels available because certain peripheral devices, for example a group of magnetic tape units, may be connected to one interface channel via a common control unit.
In addition to the already extensive range of peripheral units developed for the 1900 Series, further low-cost units have also been developed specifically to match the performance of the 1901. In particular, a new medium capacity magnetic tape system has been devised. This employs "cassette" storage that provides greater protection for the magnetic tape, thus greatly eliminating the need for expensive air conditioning, and providing far easier loading and unloading.

1902 and 1903 Processors: Capable of operating with single or dual programming Executive control, these processors can drive large numbers of peripheral devices with maximum simultaneity. They can be specified with communications facilities and therefore work in real time. The 1902 has 4,096, 8,192, 16,384 or 32,768 words of core store with a cycle time of 6 microseconds. The 1903 has 8,192 or 16,384 words with a cycle time of 1.8 microseconds or 32,768 words with a cycle time of 2 microseconds.
These processors are equipped with up to eight standard interface channels. A multiplexor unit could handle up to 63 communications lines.

Extended Mathematical Units: To provide on the 1901, 1902 and 1903 the high speed mathematical computing facilities more usually associated with the larger central processors, I.C.T. has developed special units that can be fitted and/or floating point arithmetic circuits and replace the slower extra-code facilities provided by the Executives. When one of these units is fitted no reprogramming is required, the appropriate unit being automatically used instead of the extra-code. In this way the speed of arithmetic can be measured by up to 90 times.

1904 and 1905 Processors: These are multi-programming machines and can handle up to four main programs, each with two sub-programs, at the same time. There is automatic protection against programs corrupting one another, and "Executive" allocates priority to the different jobs in accordance with the instructions of the operator. The 1904 and 1905 processors are available with 8,192, 16,384 or 32,768 words of 2 microseconds core store, and can accommodate 18 general channels, for devices such as paper tape and card equipment, and 5 fast channels, for fast peripherals such as magnetic tapes and discs. The 1905 has an autonomous floating point unit which works concurrently with other functions of the processor.

1906 and 1907 Processors: These are also multiprogramming machines and have faster processing units than the 1904 and 1905. They handle up to 16 main programs each with 3 sub-programs, with full

program protection and priority allocation.
They have core stores of 32,768 words which can be incremented to 262,144 words with a core store cycle time of either 2.1 or 1.1 microseconds. 1906 and 1907 have 18 general channels via standard interface and may be specified with as many fast channels as may be required.
A further enhancement to the productivity of the 1906 and 1907 is a choice of one or more store access controls which improve processing performance to an even greater extent. The 1907 has an autonomous floating point unit, which works concurrently with other functions of the processor.

Wide range of peripheral devices

Data Input

Punched Cards : 80 column card readers operate at 300 and 900 cards a minute. 40 column card readers operate at 600 cards a minute.
Paper Tape: Readers operate on 8 track paper tape, using the ISO 7 data bit code (5, 6.7 track may also be used), at 1,000 or 300 characters a second.
Magnetic Ink Character Recognition: The I.C.T. 8500 document sorter/reader reads magnetic ink encoded data and can sort documents at a speed of 1,200 a minute.
Universal Document Transport: This device can read mark coded documents in a range of size. Future variants will also be able to read ISO B fount alpha-numeric characters.

Data Output

Punched Cards: 80 column card punches operate at 33,100, 300 and 350 cards a minute.
Paper Tape: Paper tape punches operate at 110 characters a second.
Line Printers: Printers with 96,120 or 160 characters to the line operate at 300 or 600 or 1.350 lines per minute.

FILE STORAGE

Magnetic Tape
The magnetic tape systems are to international standards and operate at 20,800, 41,700, 60,000 or 96,000 characters a second.
Four-deck, cassette loaded, magnetic tape operates at 10,000 characters a second.

Direct Access Storage
I.C.T. provides a wide selection of direct access stores.
Magnetic Drum: Three sizes of magnetic drum provide capacities of 131,072, 524,228 or 2,097,000 characters each. Up to four drums maybe linked to one Control.
Exchangeable Disc Stores: These comprise a number of disc transports. Each transport may be loaded by the operator with a disc cartridge, which comprises six discs with a capacity of 4,090,000 or 8,190,000 characters. The average access time is 97.5 milliseconds and the data transfer is 208,000 characters a second.
Fixed Disc Stores: Three versions are available, providing a capacity of 100,600,000, 218,400,000 or 419.400,000 characters. The average access time is 152.5 milliseconds and the transfer rate is 150,000 characters a second.

Magnetic Card File: Interchangeable magazines of magnetic cards give storage for 340,000,000 characters to each file unit. There can be multiple files in the 1900 system giving a maximum capacity of 5,400,000,000 characters. The average time to select a card is 393 milliseconds. Transfer rate between the file and central processor is 80,000 characters a second. Each file unit contains 8 magazines and each magazine stores over 40 million characters.

DISPLAY DEVICES

The cathode-ray tube (CRT) display presents the contents of any part of the storage as letters, figures or symbols on a display screen, which may be situated at a distance from the computer. It permits the display of vectors and graphical data and has light pen and 35 mm. camera options available, the latter operating at 20 frames per second. A further method of display is available in a range of graph plotters either 12" or 31" wide with step sizes of either 5 or 10 thousandths of an inch. Speeds are either 12 or 18 thousand steps per minute along either axis.

COMMUNICATIONS FACILITIES

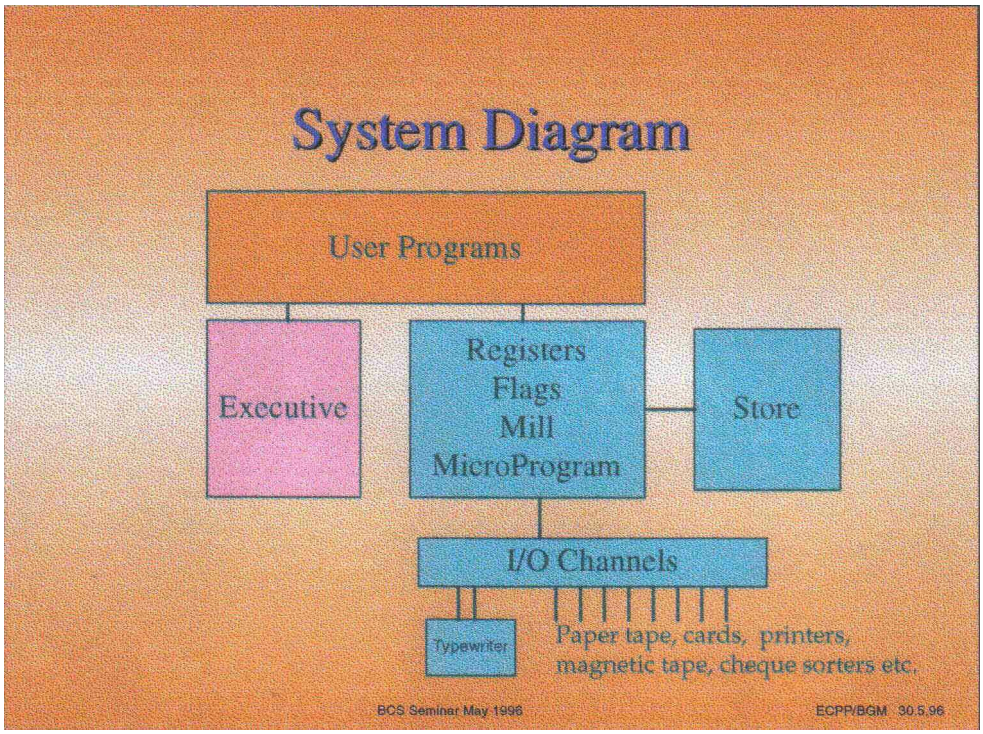
These allow a wide choice of transmission speed and type of communications circuit. Processors can be connected to one another remotely or within the same installation and can communicate with a variety of remote peripheral devices for data collection and distribution, and for interrogation of file data.”

1.3-ICT 1900 Range Architecture

The ICT 1900 compatible range relied on two key components to achieve its aims of hardware modularity and program portability.
The **ICT Standard Interface**, specified by ICT and RCA, besides providing enhanceability and flexibility to the customer, had the additional benefit of establishing a "firewall" between processor design and peripheral design, and made it very much easier to manage interfaces between development elements.
The **1900 Executive**, already present in the FP6000 architecture, was used by the ICT designers to maintain across all processors a tight and comprehensive **compatible programme interface** that was strictly controlled, and maintained by the "Compatibility Committee".
Additionally, Executives provided basic features for loading and running jobs, thus allowing 1900 machines to be delivered without Operating Systems (This gave ICT a competitive advantage in early deliveries at a time when Operating Systems complexity, development costs and timescales had been underestimated by most computer manufacturers).

1.3.1 – System Architecture

System Diagram

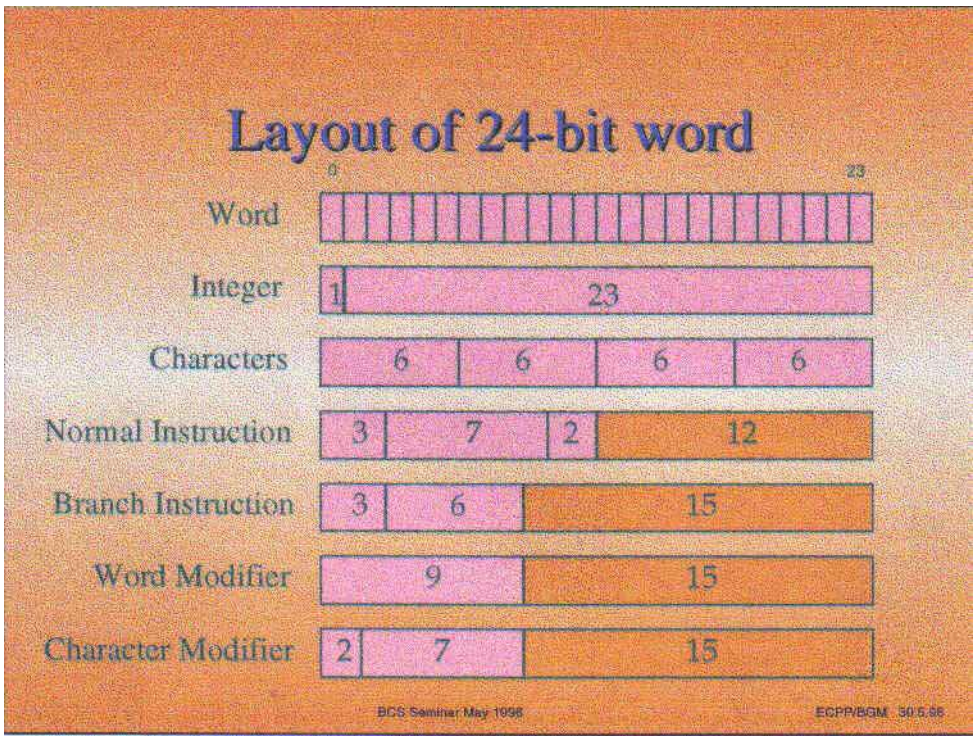


The above diagram shows the main components of the system and the relationships between them.

A user program sees instructions, which individually are executed by either the processor hardware or by executive. The user need not be aware of whether a particular instruction is carried out by hardware or Executive, and indeed it may well be implemented differently on different machines in the Range (or on different releases of the same machine). The instructions implemented by Executive are known as 'Extracodes'. When the hardware detects an instruction that needs to be carried out by Executive, it interrupts the flow of the program and transfers control to the Executive routines. When Executive has performed the required operation, control is returned to the user program at the instruction after the one that caused the interruption.

A peripheral input/output instruction is always carried out by Executive, which initiates the required operation and then returns to the program whilst the actual I/O takes place. At the end of the I/O operation the peripheral raises a Program Interrupt request, which causes the currently running program to be interrupted (which incidentally may not be the one that requested that I/O) and Executive to be entered to carry out final housekeeping, including signalling to the requesting program that the operation has completed. Control is then returned to the interrupted program.

Word Formats



The RAM (which at that time was mainly core store) held *24* bit words, with a 25th parity bit. The Bits of the word were numbered from the MOST significant end 0 to 23. A word could contain different types of information, the most important of which are shown in the above diagram and are a signed integer, up to 4 six-bit characters, program instructions, and word or character modifiers. For integers 2s complement arithmetic was used, so an integer had the top bit - bit 0 - treated as 'worth' minus two to the twenty third power. Fractions, mixed numbers, floating point and multilength numbers were also defined.

Note particularly the lengths of the N fields (shaded orange in this figure).

Program environment

The user program saw a consecutive set of 24-bit words numbered from 0 upward. Words 0-7 were known as the *accumulators* , which were addressable by the X field of an instruction. Words 1,2 and 3 could also act as modifiers addressable by the M field of an instruction (0 in the M field indicating no modifier). The contents of the modifier register were added to the N field to produce the required address. There was a maximum unmodified address of 4095 as there are only 12 N bits (except in jump instructions which have 15 N bits), from which it follows that the last directly addressable data word is in location 4095 (and the last instruction possible is in 32767). Using address modification the modified address was of 15 bits, and hence addresses up to 32767 could hold data provided it was accessed via modified instructions. The other field in a modifier was a counter, which could be used in certain instructions to increment the N field and count down, and thereby facilitating access to a set of consecutive addresses
The function bits were decoded to select the usual functions such as copy, clear, add, subtract, shift etc.. Jumps with testing of the carry, sign and overflow of the last operation, unconditional jumps, and counter / modifier jumps were also provided. Counter/modifier jumps incremented the modifier, decremented the counter and jumped if the counter was then zero; they were used to generate a program loop which progressed through an area of store defined by the starting address and the counter value.
Further functionality through a set of Extracodes which behaved, to the object program, exactly like hardware implemented instructions performed operations such as assigning peripherals, performing data transfers and sending messages to the operator. These extracodes were assigned normal function numbers, which the hardware turned into an interrupt into the Executive program. In some cases instructions that were carried out by hardware on the larger machines in the Range were implemented as an Executive Extracodes on the smaller systems (multiply and divide were done in this way on the 1902 and 1903 for example). When an extracode was encountered the user program was suspended, and its order number (the address of the current instruction) and flags (overflow, carry etc.) were dumped in word 8 of its own core store area, and control was transferred to Executive's entry point. Executive mode was set on entry which extended the hardware order code to allow executive direct hardware control over the peripherals, datum and limit registers etc.

Multi-programming and Protection

Because the machine was intended to run several user programs 'concurrently' it was necessary to provide a means of ensuring that the programs did not interfere with each other (nor with Executive) regardless of which programs they were or in which order they were loaded. This was achieved by adding a datum to each (modified) address and checking that the result did not exceed a limit defined by the declared program size. This process was carried out for every execution of every instruction, using additional hardware, the reservation checker, to keep the speed penalty down. Provided that Executive allocated each program a unique area of store delimited by the datum and limit registers there was no possibility of one program interfering with the store of another program, or Executive. Executive itself ran with a datum of zero and no limit, so the Executive code had to be 'trusted'.

The datum and limit mechanism means that programs were operating in a virtual environment (addresses are relative to the datum not to real store address zero). This means that they could easily be moved in the core store, which is a necessary requirement for multiprogramming store management. When a program was moved it was only necessary to adjust the datum register accordingly and the program could continue unchanged.

The other possible area of interference between programs would be through the peripherals. These were allocated to programs (on request) by Executive and assigned to symbolic channel identifiers so that the program need not know which particular device it was using. Of course, Executive would not allocate the same device to two programs! In addition Executive ensured that the area of store into/from which a program requested data transfer, was within that program's allocated region, and it set the hardware register that controlled the actual I/O transfer. The actual data transfers were done by a hardware mechanism called the *Hesitation System*. When a peripheral was ready to transfer a character (or word), it raised a hesitation request line, which caused the hardware to briefly hesitate from processing an instruction to allow the special hesitation hardware to steal a store cycle to transfer the character (word) into the area designated by Executive.
Peripherals were attached to each processor via the ICT (later ICL) Standard Interface. This meant that any peripheral could be attached to any member of the 1900 Range, and all peripherals had a generic similarity which simplified Executive and peripheral design. The use of the Standard Interface also meant that a particular customer could upgrade his central processor to a higher member of the Range and at the same time keep all his existing peripherals.

Extended Addressing
An early enhancement of major significance was removing the 15 bit addressing limitations imposed by the original bit assignment of the instruction word. Core stores of 16k words/module were already available and larger modules were promised imminently. This change was achieved by adding the Extended Addressing and Extended Branch modes to the architecture. These allowed 22 bit addresses through modification and indirection. Hence, in theory, core storage of up to 4 million words (16 mega characters) could be used by a user program

1.3.2- Standard Interface

The purpose of the S.I., which was totally achieved, allowed any peripheral to connect to any processor in the 1900 range. This enabled peripherals to be added or upgraded without changing the processor and, equally, for the processor to be changed to another in the range whilst keeping the peripherals. Three areas were standardised.

1. The cabling was fitted with pins and the processor with sockets; a certain cable type and 75-way plug and socket were specified after extensive testing of alternatives.

2. The signals passing between the peripheral and the processor were exactly defined in terms of pin number function and timing. The commands from the processor and the status responses from the peripheral were 6-bit items. Signal lines from the processor include an A-line to select the peripheral, an L-line to indicate the limit of the transfer and so on. Those from the peripheral were signals like Data Request (R) and Interrupt (B).

3. The electrical interface was exactly specified. The specification recommended that the same interface circuit boards were used in all the processors and the same boards in all the peripherals. This greatly reduced development effort and spares holdings.

Together with the Executive Standard Interface, software applications were fully portable across the range regardless of the processor or any specific printer, tape drive or disc system.

The 1964 specification which applied to the early 1900s provided two sets of timing rules. The lower speed catered for data rates up to a maximum in the region of 1.5 Mb/s.
The higher speed became necessary as faster discs became available and was introduced in 1967.

1.3.3- 1900 Executive

Executive was fundamental to the 1900 range concept. Together with the hardware, Executive provided the run time environment to applications and other software. It managed short-term time sharing between programs and peripherals and between programs on multiprogramming systems. It carried out peripheral transfers for programs, hiding hardware details and managing the real time interruptions. It controlled program use of store, inter-program protection and the switching between programs. On the early small systems Executive even provided by software some of the more complex instructions such as multiplication and division.

Executive was not one program. Many widely different designs were created over the life of the 1900 series, ranging from that enabling a single user program to be controlled by handswitches on a small 1901 to the later large multiprogramming overlaid Executives. Further, to minimise its use of core store, the specific Executive for a particular machine was tailored to that specific configuration.

The range interface was defined as that provided by hardware and Executive together. This enabled program portability across the range to an extent unique at the time – and in some respects not even achieved today. The same program would run unchanged on any machine and under any 1900 operating system – from the smallest machine running under Executive alone to the largest running under the powerful George 3 or George 4 operating systems. (This contrasted with the IBM 360 series where the interface was defined at the hardware level and some program changes could be required when moving from one regime to another.) The use of the "extracode" technique was a key factor: instructions such as those used to drive peripherals would appear to a user program as part of the order code but in fact be carried out by software in Executive.

Executive was managed as part of the hardware, the development teams reporting to the hardware management and support being provided by Customer Engineering Services. The position of the range interface and the development teams being together enabled different mixes of hardware and software to be created, as appropriate to the specific system requirement.

Compatibility of this interface was absolute for a program moving to a system up the range, or when moving forward in time to a later machine or to a later version of Executive. Downward compatibility was also strict for a program not using facilities only available higher up in the range. Moreover null responses were normally provided for a such facility when not present- so enabling that to be detected and alternative action taken. Strict compatibility carried through to the later DME systems, which enabled 1900 software to be run on 2900 machines.

The interface definition was controlled by a Compatibility Committee which was formed in 1964 spontaneously between the active parties. There was more willingness to compromise between designers than is often the case – in part because the original architecture was imported from outside so no-one's sacred cow! This committee also controlled file formats for magnetic media.

Complex job management on 1900 systems was provided by the George operating systems which ran on top of Executive. However Executive provided basic features for loading and starting programs and so a 1900 machine could be used without any George system. This enabled a small machine without any disc or drum (backing store) to be run without the overhead of a George. It was also invaluable early on in enabling systems to be delivered before development of the George systems was complete.

George 1 and 2 used the normal user interface to Executive. (Later, on small disc systems George 1 facilities were eventually merged into an Executive variant known as George 1S.) George 3 and 4 systems were much more complex. Here Executive was a smaller core, insulating George and other programs from the hardware. A special interface existed between George and Executive and the two worked together to provide the full range interface to the programs above.

1.3.4 – The 1900 Range Order Code

The following is an extract from the 1900 Plan Manual, detailing part of the range compatible order code visible to the 1900 programs.

1900 Series PLAN Summarised Programming Information

ICL

000	LDX	$x' = n + c$	V
001	ADX	$x' = x + n + c$	V
002	NGX	$x' = -n - c$	V
003	SBX	$x' = x - n - c$	V
004	LDXC	$x' = n + c$	C
005	ADXC	$x' = x + n + c$	C
006	NGXC	$x' = -n - c$	C
007	SBXC	$x' = x - n - c$	C
010	STQ	$n' = x + c$	V
011	ADS	$n' = n + x + c$	V
012	NGS	$n' = -x - c$	V
013	SBS	$n' = n - x - c$	V
014	STOC	$n' = x + c$	C
015	ADSC	$n' = n + x + c$	C
016	NGSC	$n' = -x - c$	C
017	SBSC	$n' = n - x - c$	C
020	ANDX	$x' = x \,\&\, n$	
021	ORX	$x' = x \vee n$	
022	ERX	$x' = x \neq n$	
023	OBEY	Obey the instruction in N	
024	LDCH	$x' = n_j$	
025	LDEX	$x' = n_e$	
026	TXU	Set C if $n \neq x$ or $c = 1$	
027	TXL	Set C if $n + c > x$	
030	ANDS	$n' = n \,\&\, x$	
031	ORS	$n' = n \vee x$	
032	ERS	$n' = n \neq x$	
033	STOZ	$n' = 0$	
034	DCH	$n_j' = x_3$	
035	DEX	$n_e' = x_e$	
036	DSA	$n_a' = x_a$	
037	DLA	$n_m' = x_m$	
040	MPY	$x{:}' = n.x$	V
041	MPR	$x' = n.x$ rounded, $x^{*\prime}$ spoiled	V
042	MPA	$x{:}' = n.x + x^*$	V
043	CDB	$x{:}' = 10.x{:} + n_j$	V
044	DVD	$x^{*\prime} = x{:}/n$, x' = Remainder	V
045	DVR	$x^{*\prime} = x{:}/n$ rounded, x' = Remainder	V
046	DVS	$x^{*\prime} = x^*/n$, x' = Remainder	V
047	CBD	$x{:}' = 10.x{:}$, n_j' = Character	

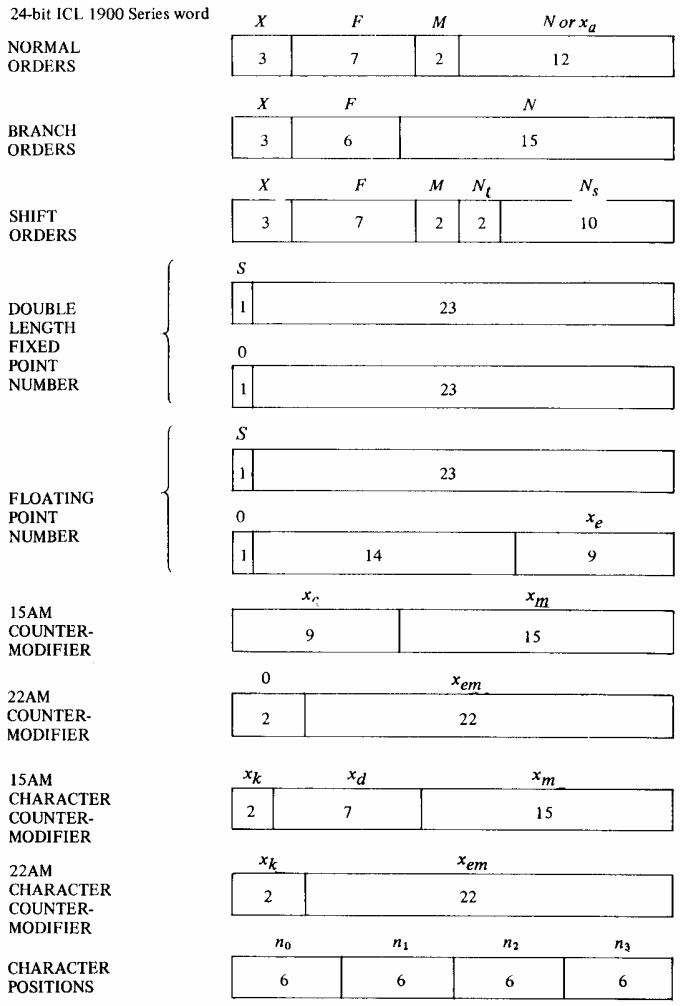
050	BZE	Branch to N if $x = 0$	
052	BNZ	Branch to N if $x \neq 0$	
054	BPZ	Branch to N if $x \geqslant 0$	
056	BNG	Branch to N if $x < 0$	
†060	BUX	Single word modify: $x_m' = x_m + 1$	$x_c' = x_c - 1$
†062	BDX	Double word modify: $x_m' = x_m + 2$	Branch to N [if $x_c' \neq 0$]
†064	BCHX	Character modify:	
		$x_k = 0, 1$ or 2 $x_k' = x_k + 1$, $x_m' = x_m$	$x_d' = x_d - 1$
		$x_k = 3$ $x_k' = 0$, $x_m' = x_m + 1$	Branch to N if $x_d' \neq 0$
*066	BCT	Count least significant 15 bits of X.	$x_m' = x_m - 1$
			Branch to N if $x_m' \neq 0$

	070	CALL	Subroutine Entry	
			Link in X	
	072	EXIT	Subroutine Exit	V
			Link in X	
	074		Conditional Branch to N:-	
$X = 0$		BRN	Branch unconditionally	
$X = 1$		BVS	Branch if V is set	
$X = 2$		BVSR	Branch if V is set and clear V	
$X = 3$		BVC	Branch if V is clear	
$X = 4$		BVCR	Branch if V is clear or clear V	
$X = 5$		BCS	Branch if C is set	
$X = 6$		BCC	Branch if C is clear	
$X = 7$		BVCI	Branch if V is clear and/or invert V	V
	*076	BFP	Test floating point accumulator or floating point overflow, and branch accordingly.	
		$X = 0$	Branch to N if $a = 0$	V
		$X = 1$	Branch to N if $a \neq 0$	V
		$X = 2$	Branch to N if $a \geqslant 0$	V
		$X = 3$	Branch to N if $a < 0$	V
		$X = 4$	Branch to N if FOVR is clear	
		$X = 5$	Branch to N if FOVR is set	
		A remains unchanged.		

	100	LDN	$x' = N + c$		
	101	ADN	$x' = x + N + c$	V	
	102	NGN	$x' = -N - c$		
	103	SBN	$x' = x - N - c$	V	
	104	LDNC	$x' = N + c$		
	105	ADNC	$x' = x + N + c$	C	
	106	NGNC	$x' = -N - c$	C	
	107	SBNC	$x' = x - N - c$	C	
$N_t = 0$	110	SLC	Shift x left N_s places. Circular		Single length
$N_t = 1$		SLL	Shift x left N_s places. Logical		
$N_t = 2, 3$		SLA	Shift x left N_s places. Arithmetic	V	
$N_t = 0$	112	SRC	Shift x right N_s places. Circular		
$N_t = 1$		SRL	Shift x right N_s places. Logical		
$N_t = 2$		SRA	Shift x right N_s places. Arithmetic		
$N_t = 3$		SRAV	Shift x right N_s places. Special		
	*114	NORM	Normalize x	V	
	*116	MVCH	Transfer N characters		
$N_t = 0$	111	SLC	Shift $x{:}$ left N_s places. Circular		Double length
$N_t = 1$		SLL	Shift $x{:}$ left N_s places. Logical		
$N_t = 2, 3$		SLA	Shift $x{:}$ left N_s places. Arithmetic	V	
$N_t = 0$	113	SRC	Shift $x{:}$ right N_s places. Circular		
$N_t = 1$		SRL	Shift $x{:}$ right N_s places. Logical		
$N_t = 2$		SRA	Shift $x{:}$ right N_s places. Arithmetic		
$N_t = 3$		SRAV	Shift $x{:}$ right N_s places. Special		
	*115	NORM	Normalize $x{:}$	V	
	*117	SMO	Supplementary modifier to next instruction		

120	ANDN	$x' = x \,\&\, N$
121	ORN	$x' = x \vee N$
122	ERN	$x' = x \neq N$
123	NULL	No operation
124	LDCT	$x_c' = N$, $n_m' = 0$
125	MODE	Set zero suppression mode
126	MOVE	Transfer N words from address x to address x^*
127	SUM	x' = Sum of N words from address x^*
* 130	FLOAT	Convert n: from fixed to floating and store in A
* 131	FIX	Convert a from floating to fixed and store in $N(M)$ and $N(M) + 1$
* 132	FAD	$a' = a + n$:
* 133	FSB	$a' = a - n$: For $X = 0$, as shown
* 134	FMPY	$a' = a.n$: For $X = 4$, interchange a and n:
* 135	FDVD	$a' = a/n$:
* 136	LFP	$a' = n$:
* 136	LFPZ	$a' = 0$, when $X = 1$
* 137	SFP	$n' = a$
* 137	SFPZ	$n' = a$, $a' = 0$, when $X = 1$
150	SUSBY	Suspend if a specified peripheral is active
151	REL	Release a specified peripheral
152	DIS	Disengage a specified peripheral
153		Unassigned
154	CONT	Read more program from a specified peripheral
* 155	SUSDP	Suspend and dump program on a specified peripheral
156	ALLOT	Assign, or supply information about, a specified peripheral or file.
157	PERI	Initiate action on a peripheral according to control area N(M)
160 0 N(M)	SUSTY	Suspend and type message on console typewriter
160 1 N(M)	DISTY	Type message on console typewriter without suspension
160 2 N(M)	DELTY	Delete program and treat message as console directive
161 0 N(M)	SUSWT	Suspend and type HALTED n_a (as two characters) on the console typewriter
161 1 N(M)	DISP	Type DISPLAY n_a (as two characters) on the console typewriter without suspension
161 2 N(M)	DEL	Delete program and type DELETED n_a (as two characters) on the console typewriter
* 162 X N(M)	SUSMA	If $n^* = 0$, make $n^{*\prime} \neq 0$ and $n' = x$, and omit next instruction. If $n^* \neq 0$, proceed to next instruction.
* 163 X N(M)	AUTO	Activate member X at N(M). For reactivation, N(M) must be zero.
* 164 1 0	SUSAR	Suspend current member awaiting reactivation by AUTO.
* 164 2 0	SUSIN	Suspend current member awaiting flag-setting interrupt or AUTO.
165 X N(M)	GIVE	N(M) = 0 Give date in binary in X N(M) = 1 Give date in characters in XX* N(M) = 2 Give time in characters in XX* N(M) = 3 Give current core store allocation in X. N(M) = 4 Alter core store allocation to that specified in X. N(M) = 5 Give details of Executive and central processor N(M) = 8 Give current address mode and branch mode in X N(M) = 9 Alter address mode and branch mode to those specified in X
* 166 X N(M)	RRQ	X = 0 Read request block into store at N(M) X = 1 Replace request block from store at N(M)

24-bit ICL 1900 Series word



Notes

The function codes 140 to 147 are undefined

C These instructions may set the carry register but cannot cause overflow. The 043 order may set V or C.

The carry register C is left clear by any order except 023, 117 and 123, unless that order sets C.

V These instructions may cause overflow.

* These instructions are not available with some machines or with some Executives.

For the availability of instructions with particular machine configurations see the Central Processors manual.

† In 22-bit address mode these instructions operate on X_{em} instead of x_m and branch unconditionally to N.

This card does not in all cases give a complete definition of an instruction. Further information on each instruction may be found in the Central Processors manual and the Plan Reference Manual. Hardware and software developments may alter the specifications of some instructions subsequent to the date of going to print, so a close watch on User Notices and relevant manual amendments is recommended.

Branch instructions are defined here in direct branch mode terms only. For extended branch mode, please refer to the Central Processors manual or the PLAN Reference Manual.

1.3.5 – FP6000 Processor Data Flow

This extract from the April 1963 visit report details the dataflow of the FP6000 processor being recommended for adoption. It later became the ICT 1904.

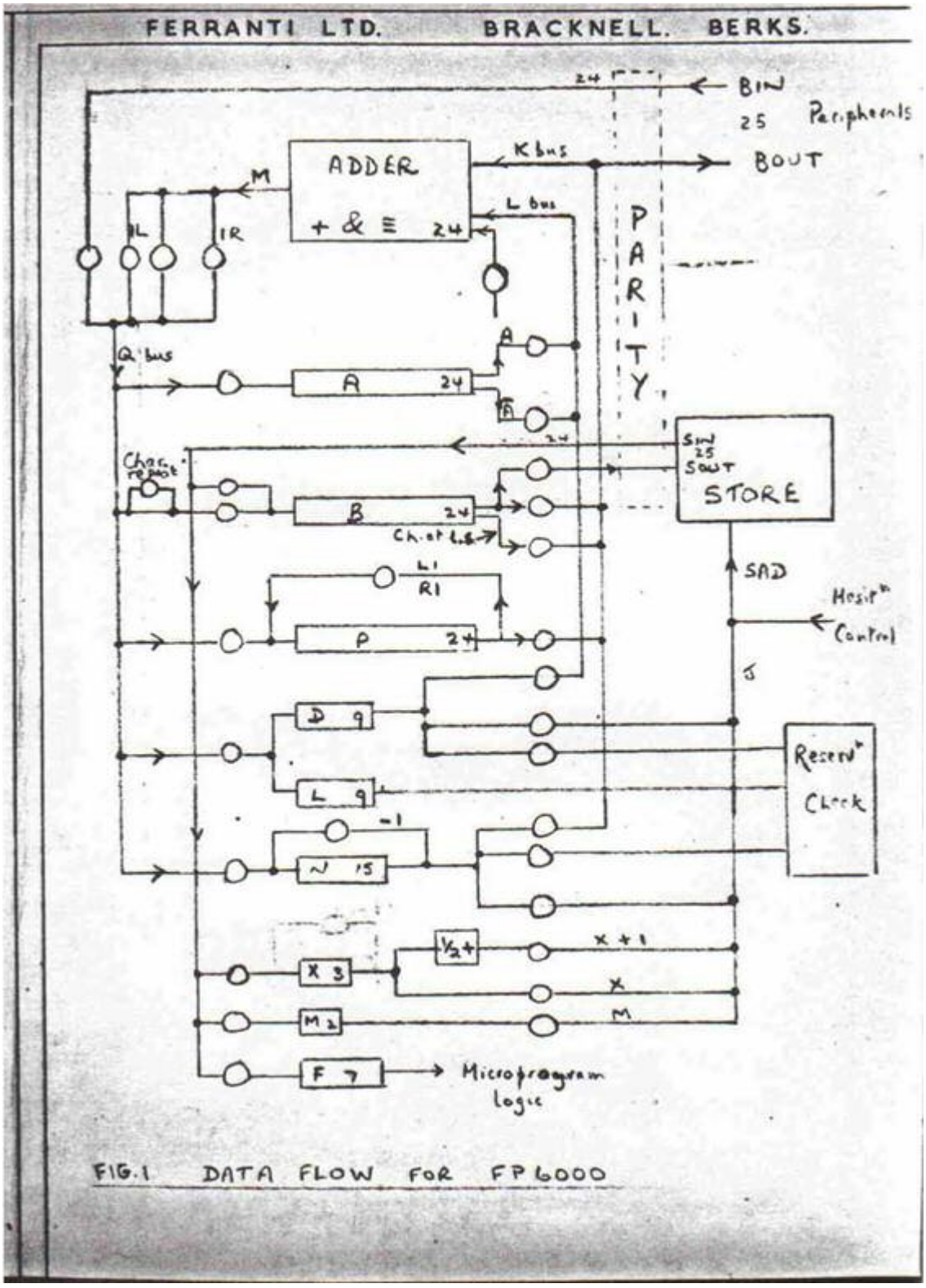


FIG.1 DATA FLOW FOR FP6000

Data Flow

General – The above figure shows the main FP6000 data flow which is relatively straightforward. One unusual feature is the dumping of the order number register P into store during all double length operations (including multiply, divide and floating point).
Briefly the data flow consists of a mill (+, &, ≠) with 2, 24 bit parallel input highways and one 24 bit output highway. The latter emerges via a shift facility (0, +1,-1). The accumulators are not external but held in the core store. The L input highway serves A, a 24 bit working register with output complementing facility for subtraction, D, a 9 bit register holding the datum for that programme (see time sharing below). The K input highway serves B, the core store data register, P, the order number register which is also used for double length numbers and N, a 15 bit register holding the store address. P has a shifting facility (+1,-1) for use in multiplication and division.

Store addressing and data
The store is addressed for instructions, operands (N), accumulators (X) and modifiers (M) all relative to the datum D for that programme which is added to all N addresses but ORed to X and M (See below). A further facility is provided for addressing the store with X+1 for double length quantities. Data into and out of the store is via the B register which is actually the store data register. The latter is not part of the memory as is usual. This assists considerably in simplifying store expansion. Similarly, N, is the store address register. All data transfers to and from store are checked by a 24 bit parity generator/ checker which also checks peripheral transfers over the standard interface.

Multiprogramming (Time Sharing)

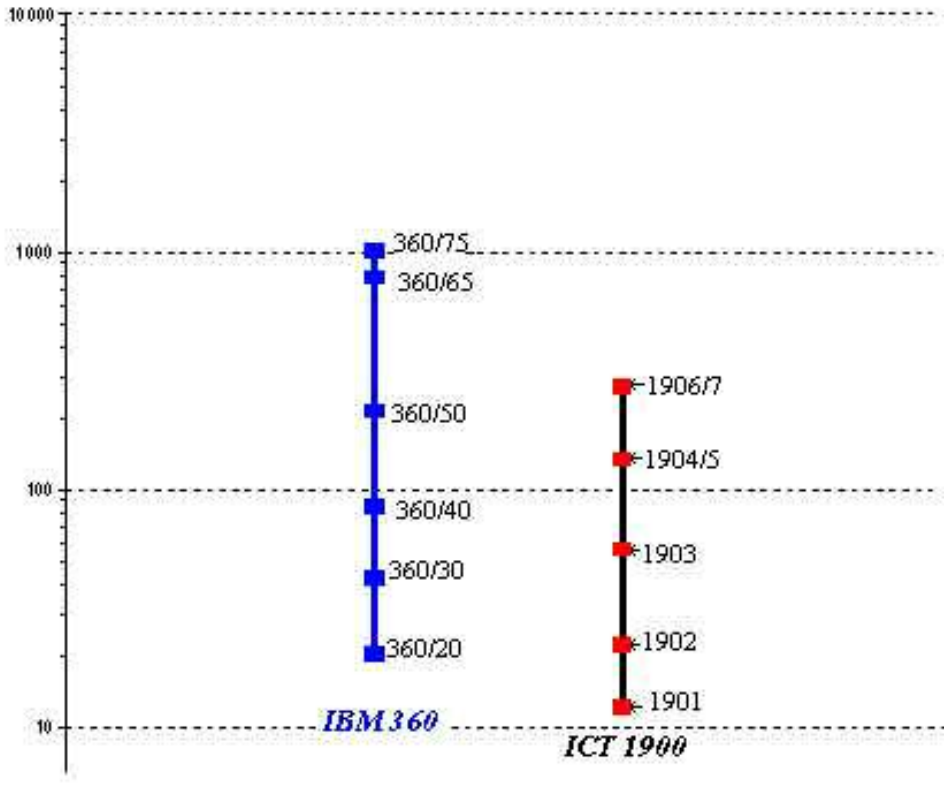
A hardware facility provides a reservation check that the address N (modified by M if required) is less than or equal to L and adds the datum B to N. This ensures that all store accesses lie between D and D+L. D and L are set by the EXECUTIVE (Supervisor). Both D and L are modulo 64.

1.3.6 - Span of the Range

The brilliant simplicity of the original FP6000 design and the design skills of the ICT engineers made it relatively easy to expand the design into a series of systems spanning a wide range of performance and price. Unsurprisingly, the greater difficulty was encountered in expanding the range upwards.

The 1906/7, the top model of the original series, had a performance that was significantly below the upper models of the 360 range, and this led to the early introduction of dual processors.
Anonymous dual processors (1906/7E/F) shared the same IAS (core store) via one or more SMAC's (Store MultiAccess Control) and ran two (or more) programs concurrently without them being aware of each other, under the control of a single operating system. Given a suitable workload, a dual processor could reach almost double the performance of a single.
The multiprocessor design was extended in the 1908 (a four processors system), unveiled at the Edinburgh IFIP in 1968, but overtaken by events and not put into development.
The perceived need to have more powerful single processors to compete more effectively in an area of the market where new advanced applications (such as large real time transaction processing) were emerging, was one of the many factors leading, eventually, to the top down introduction of the 2900 Range in 1974

At the lower end of the range, immediately after the 1901, a system below 1901 was seriously investigated. Initial feasibility studies proved that it was technically feasible to design and manufacture a 1900 compatible system at the right cost and suitable specification. But, given the selling methods used at the time, the selling costs made such a system unprofitable, and the project was dropped.
The viable span of the range (1901-1906/7) was thus established.
.
The following chart plots the commercial performance of each (single) processor in the ICT 1900 and IBM 360 in1966, measured by instruction mixes (POWU2/sec., see 2.3), and the span of each range.



1.4 - Hardware technology in the ICT/ICL 1900 Range

This section outlines the technology changes which took place during the lifetime of the 1900 and traces some of their impacts on machine specifications and design. Like most successful product ranges the 1900s exhibited a mixture of innovative leaps forward followed by periods of consolidation and evolution. Initially in contrast to today's position ICT had to do almost everything itself. ICT engineers selected circuit families, designed the Printed Circuit Board (PCB) technology for mounting and connecting the logic circuits then the next level of connection between the boards and finally the cabling, power, cooling and cabinets to make up the complete processor product.

Design tools were needed to aid the designers and to present information to manufacturing. Over the period of the 1900 series there was a great increase in the complexity of the design process made possible by a continuing investment in design tools. Manufacturing faced various challenges. Technologies demanded increasingly complex structures with tighter tolerances. At the same time volumes increased tenfold and average product costs reduced by perhaps threefold. It is a tribute to the skill and dedication of the designers that such an undertaking could be sustained by a relatively small workforce in comparison to our competitors.

Deliveries started in 1965 and continued until it was superseded by the 2900 series in the 1970s. There were five sub-series - the original, E&F, A, S and T. The 2903/2904 and ME29 were derivatives of the 1900. The initial priority was to expand the FP6000 and to introduce a broad range of systems quickly. The technology chosen was a derivative of that used for FP6000. This technology was an evolution of that previously used by Ferranti and was robust and well understood. The circuits were based on the FP6000 but used more reliable silicon transistors. The PCBs were simple with two-sided tracking and without plated through holes to interconnect the sides. The logic design was done manually. The wiring design for the 1902 used a CAD system which ran on the EMIDEC 2400. The backplane was connected using direct point-to-point wiring. Wires were pre-cut to standard lengths. To make the wiring process semi-automatic, a machine presented the wiring list one wire at a time. An operator on one side of the machine inserted the wire. An operator on the other side used a jig to test that the wire had been connected between the correct pins.

The Original 1900 Series

The original series built using this technology comprised the 1901, 1902, 1903, 1904 and 1906 for commercial applications, spanning a wide performance range, and the 1905, 1907 and 1909 for scientific and engineering work. The scientific machines were variants of the commercial systems with added hardware for floating point operations. The larger members of the range carried different model numbers, while the smaller members just had a feature number for the added hardware. This approach to the scientific market and the nomenclature was carried forward to subsequent members of the range.

The mid-range 1904 was the FP6000 with the 1900 Standard Interface and using silicon technology. The 1906 was a new design with hardware registers and additional data flow to boost the performance to some 50% higher than the 1904. A variant with a faster store gave a further 35% performance boost. The 1903 was a simplification of the 1904. Extracodes were substituted for expensive hardware operations, and smaller configurations were supported to give performance about 40% that of the 1904. The 1902 was a 1903 with a slower store and performance about half that of 1903. The 1901 used a serial/parallel data flow with performance 50% of the 1902.

System	First Del.	Proc. Clock ns	CORE store		I/O	
			Cycle us	Size KWs	Max no of Channels	Est. Max Rate kch/s
1907 (1µs)	1967	750	1.1	32-256	no limit	3200
1906 (1µs)	1967	750	1.1	32-256	no limit	3200
1907 (2µs)	1967	750	2.1	32-256	no limit	2000
1906 (2µs)	1967	750	2.1	32-256	no limit	2000
1909	Aug. 1965	1000	6	16-32	23	
1905	May-65		2	16-32	23	264
1904	1965		2	16-32	23	264
1903	Jul-65		2	8-32	8	340
1903 EMU*			2	8-32	8	340
1902	1965		6	4-32	8	220
1902 EMU*			6	4-32	8	220
1901	Sept. 1966	4000	6	4-16	6	220

**EMU = Extended Mathematical Unit*

Peripherals were in general connected via the 1900 Standard Interface. This made it possible to separate the development and lifespan of the peripherals from the processors and to use them on every machine in the range. Early systems offered a comprehensive range of peripherals with the exception of exchangeable discs. Many of these had long lives and continued in active use over several processor generations. Punched card readers and punches were ICT designs drawing on the company's traditional skills in card equipment. The 80-column card punch used a mechanism which was essentially unchanged from its design in 1910. The printers were also ICT designed and built. Tape transports came from a variety of suppliers including DRI (UK), C des C (France) and CDC (USA). Manufacturers of drums and fixed disc stores included Data Products and Bryant. Exchangeable discs, introduced about 1966, were from CDC and DRI.

The E/F Series

System	First Del.	Proc. Clock ns	CORE store Cycle us	CORE store Size KWs	I/O Max no of Channels	I/O Est. Max Rate kch/s
1907 E/F	1968	750	1.8	32-256		2400
1906 E/F	1968	750	1.8	32-256		2400
1905E	1967	750	1.8	32-128		1200
1905E (H/W Registers)		750	1.8	32-128		1200
1905F		750	0.75	32-128		1200
1904E		750	1.8	32-128		1200
1904E (H/W Registers)		750	1.8	32-128		1200
1904F		750	0.75	32-128		1200

The first development was the E/F series - the 1904E, 1905E, 1906E, 1907E and the similarly numbered F machines. It used the same technology as the original 1900s with several architectural improvements. The extended addressing modes introduced with the 1906 were applied to the upper half of the range, allowing programs (and their data) larger than 32K words, reinforcing the requirement for the larger physical stores which were offered.

Dual processors were introduced. The 1906E was a dual 1904E which provided increased throughput compared with the original 1906 with the additional benefits of resilience against CPU failure and the ability for customers to upgrade from installed 1904Es. A 1904E was used to develop the 1900 paging feature which was incorporated in the large A-series machines.

The E/F series was a mini-range centred on a single design core. Variants included optional hardware registers for the accumulators (20% performance gain), alternative stores of 2µs and 1µs (the difference between E and F worth about 25%), a floating point unit and dual processors as mentioned above. The economies in development of this approach yielded benefits in price and timeliness to market.

Evolution of internal control

A processor typically has to perform a sequence of internal operations in order to obey an instruction in a program. During each step in the sequence it is necessary to tell internal controls what action to take. There are typically hundreds of internal controls and their operation will depend on factors like the type of program instruction, its position in the sequence and the results so far. The implementation of these control mechanisms is a crucial part of the overall design, strongly influencing speed and cost. They can easily occupy as much as half the processor logic.

There are two main types of control schemes. In a hardwired scheme the sequences and derived controls are implemented using the standard logic family. Optimisation techniques can reduce the size, but often at the expense of increased complexity. The "microprogram store" approach regularises the controls into a single store analogous to the storage of instructions in a program.

The early machines used discrete component logic which was relatively expensive. Designing a specialised fixed store was good value where there were large numbers of controls as in the 1906/7 and the E/F series. The 1906/7 used a classical bit-mapped approach where controls are mapped directly to bit positions in the microprogram word (96 bits wide in this case).

The E/F series used a coded approach where fields in the microprogram word controlled groups of actions. The E/F store was 48 bits wide.

The A, S and T machines used Small to Medium Scale Integration (SSI/MSI) integrated circuit families. They offered cheaper logic but did not provide any fast and cheap storage components so it was more cost effective to implement hardwired control in those machines.

By the time of the 2903 and ME29, integrated circuit technology could provide memory components to hold microprograms. Their relatively low cost allowed large microprogram stores and they had the great benefit of being soft-loadable. This allowed a blurring of the distinction between low-level control microprogram functions and parts of the Executive functionality. This was used to great effect in such areas as the 2903 Direct Data Entry feature.

The 1900 A Series

System	First Del.	Processor Clock ns	CORE store		I/O	
			Cycle us	Size KWs	Max no of Channels	Est. Max Rate kch/s
1906A	1970	100	0.75	32-256		6500
1904A	1969	500	0.75	32-128		3000
1903A	1968	720	1.5	16-64	12	600
1903A SCF‡	1968	720	1.5	16-64	12	600
1902A	1968	1500	3	8-32	8	520
1902A CCF†/SCF‡	1968	1500	3	8-32	8	520
1901A	1969		4	4-16		220
1901A CCF†	1969		4	4-16		220

† CCF= Commercial Computing Feature (Group 4 instructions- Fixed Point Multiply/Divide and I/O conversion)
‡SCF= Scientific Computing Feature (Group 13 FP instructions – held FP Accumulator)

The 1900 A-series machines were a landmark as they marked the move to integrated circuit technology. By the time of their design there were two integrated circuit families with the speed required to meet the needs of the 1900s. The TTL family was pioneered by Texas Instruments and subsequently taken up by many semiconductor companies. Stevenage led the early ICT work with an experimental TTL 1900 built in 1966. Motorola had been developing the MECL2.5 range. Manchester engineers developed a novel way of using these circuits and collaboration between ICT and Motorola led to the development of the Motorola MECL10k range which was still being made in 1996.

The speed and small size of ICs forced a fundamental re-examination of the whole packaging technology. Two approaches were developed. For TTL, a modular approach to PCBs was adopted with four different board sizes. Much of the interconnection moved from the backplane to tracking on the PCB. The benefit was increased speed. The disadvantage was that there were now many board types to design and support. PCBs were four layers and had plated-through holes. The backplane was wrap-wired. For MECL10k the interconnection used "series matched transmission lines". One or two ICs were mounted on plug-in cards which contained the series matching resistors. The plug-ins were interconnected by a multi-layer platter which matched the transmission line.

The handling of the complexity of the new technologies was made possible by equally significant advances in design tools. Particular mention can be made of the tracking system used to route interconnections in the platters automatically. Handling the multi-layer boards demanded a massive jump in manufacturing capability so the PCB plant in Kidsgrove embarked on a series of process developments and investments which moved it into world-class, a position it has continued to maintain. Computers that used ICs were termed "Third Generation". ICT was among the first companies worldwide to adopt these IC technologies and turn them into products with the A-series which had the effect of moving the 1900 technology base from conservative to leading edge. TTL technology was used for the 1901A to 1904A. The fast but more expensive MECL10k was used for the 1906A.

All machines had optional floating point capability. The 1904A and 1906A had a paging capability and optional High Speed Mode I/O channels which were used to attach fast drums for this purpose. The 1902/3A machines were one processor with different stores. The 1902A used cheaper timing circuits and ran at a slower clock rate. The 1901A used a new compact design incorporating a printer in the same housing as the processor. It had a new, low cost Twin Exchangeable Disc system. To optimise performance the 1906A used a system of asynchronous timing in which the internal beat rate of the machine changed according to the operation it was performing.

The 1900 S Series and 1900 T's

System	First Del.	Processor Clock nS	Store		I/O	
			Speed uS	Size Kws	Max no of Channels	Est. Max Rate kch/s
1906S	1973	100	0.3	32-512		11000
1904S	1972	300	0.5	32-256		5000
1903S	1971	640	1.5	16-128	18	1400
1903T	1973		0.8	32-128		2500
1902S	1971	1500	3	16-64		1100
1902T	1974	1000	3	16-64		830
1901S	1971		4	8-16		235
1901T	1974		4	16-64	13	630

The S-series was the last to span the entire 1900 range. By the time of the T-series the larger machine requirements were being fulfilled by the new 2900 range. However as 2900 was being introduced with the larger models first, the lower part of the 1900 range continued to sell and was refreshed by the T-series. The S-series was a comprehensive upgrade across the range. The enhancements were all evolutionary but significant in their scale. The 1906S received a spectacularly fast store made by Plessey using plated wire technology and cycling in 250ns, more than twice the speed of previous stores, which gave it a 40% performance uplift. The 1904S made selective use of the new, faster Schottky STTL logic for a 30% performance gain. The 1903S had extended store capability and a fast peripheral scheme with more Standard Interfaces. The 1902S and 1901S grew their configurations and their throughput.

The purpose of the T-series was to keep the lower members of the range competitive. Performance upgrades were achieved by regrading higher machines; the 1903T was based on the 1904A and so on. All machines had semiconductor stores. The 1901T and 1902T had Integrated Disc Controllers to reduce costs and floor space.

The 2903 Series

The 1900 machines were positioned as what we today would call mainframes.
ICL was determined to enter a rapidly growing new segment characterised by companies which were too small to have a DP department. Computing needed to be made simpler. The 2903 range and ME29 range were developed for this segment. A robust but inexpensive architecture was needed and the elegance and simplicity of the 1900 architecture fitted the bill well. The naming, market positioning and projection of the machines distanced them from the 1900 range. From a customer viewpoint they were not 1900s. However, from an architectural and engineering viewpoint it is clear that under the Hot Tango skin there beat a 1900 heart.

The 2903 employed an evolution of the TTL technology used in the A-series. Semiconductor store components were just becoming available from Intel and it was decided to exploit them with a soft microprogrammed design. The 2903 was one of the first machines in the world to use this technology, as we became painfully aware when Intel ran into difficulties - truly the "bleeding edge". The 2903 innovations were formidable including a semiconductor main store, a semiconductor control store addressed as part of the main store, a video console compared with the teletype console of the 1900 range, Direct Data Entry in parallel with other operations, new Fixed and Exchangeable Discs, a new shape and the 2900 colour. And it was an overnight success. Later the 2904 provided a twofold power boost. The 2903 was designed with data routes capable of upgrading to eight bits for compatibility with 2900. An experimental 2900 version was developed at Dalkeith but did not go into production.

System	First Del.	Processor Clock nS	Store		I/O	
			Speed uS	Size Kws	Max no of Channels	Est. Max Rate kch/s
2903/25	May-76	540	1.14	Up to 64		
2903/40	Mar.-74	540	1.14	Up to 64		520
2904	May-76	540	1.14	Up to 96		
ME29	1980					

The ME29 succeeded the 2903 and was also a soft microprogrammed machine. It resulted from collaboration with Palyn Associates on an emulator known as Emmy using MECL technology. The model 35 had similar performance to 2904 while the 45 was 80% faster.

The 1900 range was sold over a period of more than a decade from 1964. The architecture continued in the 2903 and ME29 ranges, extending the total lifetime to some 25 years. 30 years on, orders were still being taken in 1997 for 1900 applications to run on Series 39 machines under the CME* operating system. The range was undoubtedly a success story for ICT and later ICL. While many people and groups contributed, its success owes a great deal to the skill and dedication of engineering teams throughout the company. The hardware and software product engineers, tools and support engineers and manufacturing engineers created and sustained a complete range. And they did it with a fraction of the resources employed by our main competitor.