Ferranti Atlas 1 & 2 – Systems Architecture
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1. Introduction

The **Atlas 1** computer (originally known as just Atlas) was developed by Ferranti Ltd in collaboration with the Department of Electrical Engineering at Manchester University. At its inception it was one of the most powerful systems in the world - possibly the most powerful. Its design contained a number of innovations, including an operating system - the Atlas Supervisor - which allowed simultaneous multiprogramming of user programs and a *one-level store*, whereby code and data were moved between fast main memory and backing storage in a manner invisible to individual programs. Atlas 1 used magnetic core store and drums for the two storage mechanisms, as well as a fast fixed-store of ferrite and copper rods (the so-called *hairbrushes* – see Figure 1). The latter held parts of the Supervisor and commonly-used routines, including input and output, which could be accessed by user programmers by a single instruction (an *extracode*).

Figure 1: An Atlas Fixed Store Module

Atlas 2 was developed in collaboration with the Mathematical Laboratory at Cambridge University. It was smaller, particularly in storage availability, but retained many of the features of the larger machine. Only core store was provided for program memory, together with a slave store to improve performance.

As general purpose 'scientific' (as opposed to commercial data processing) machines, Atlases were used mainly for technical work, both in the academic and research establishments that installed them and in others which were provided with remote access services. Ferranti, and later ICT, also provided a bureau service on the Manchester machine.

2. Registers & Storage

See Figure 2. [Author's note: Most figures have been lifted directly from the references, are of poor quality, and should be replaced]

Atlas has one floating-point accumulator. Floating-point numbers are 48 bits of which 8 bits form an octal exponent, but the accumulator has a double-length mantissa. There are 128 index registers or *b-lines* most of which are 24 bits long, that can also be used for fixed-point arithmetic. Some of these are special purpose - e.g. B0 is always zero; B127 is the control register and contains the address of the currently obeyed instruction. Storage words are 48 bits and may contain:
- a floating point number

- two 24-bit numbers. These are normally taken to be a 21-bit signed integer with an octal fraction
- eight 6-bit characters
- an instruction - see module **X3.**
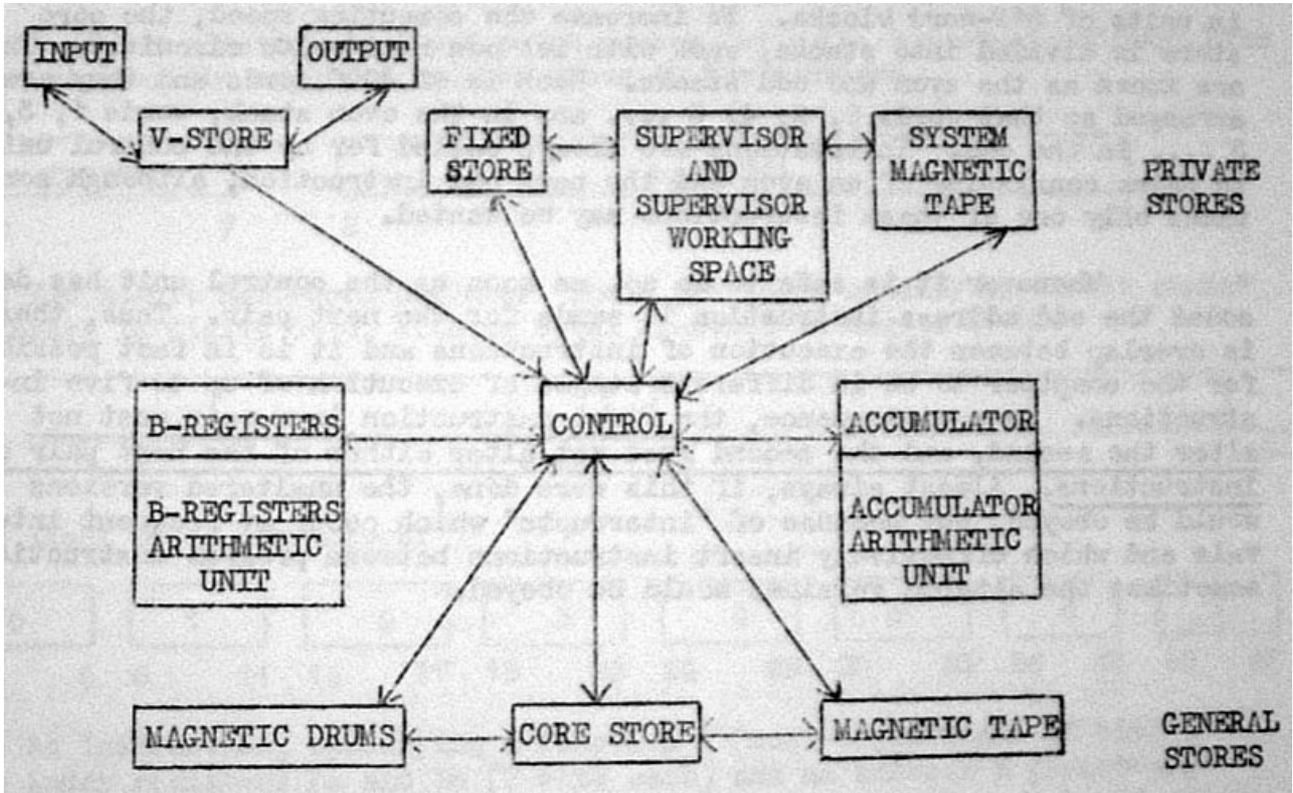
Figure 2: Atlas 1 Stores & Registers

The accumulator has an associated arithmetic unit, as do the B registers. These are independent of each other and can run in parallel.
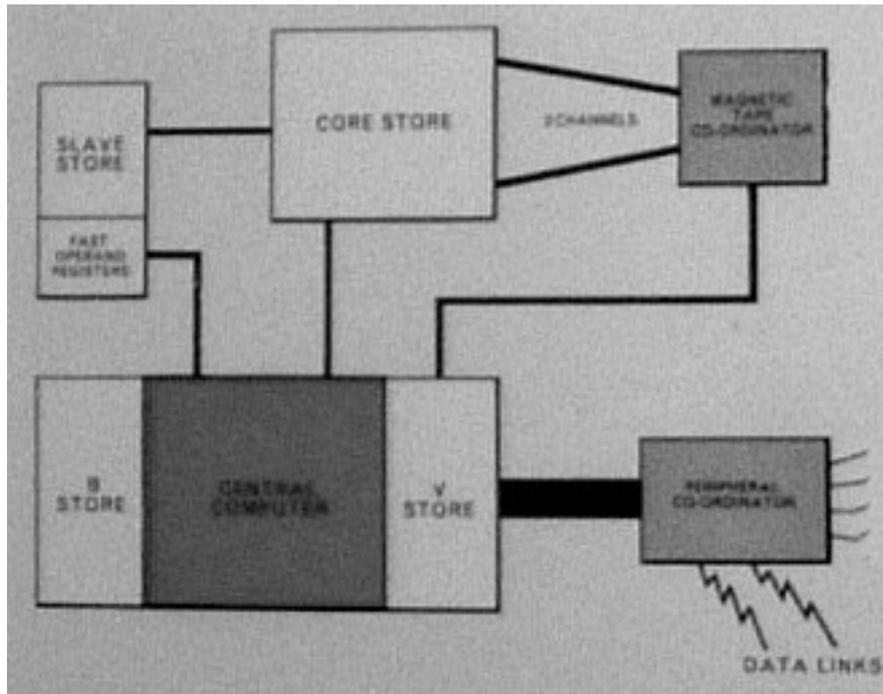
Figure 3: Atlas 2 Stores & Registers

Atlas 1 has core store, drums, a fixed store – see 1 above – and the *V store*. The V store is a collective name given to various flip-flops throughout the computer, which can be read, set, and re-set by reading from or writing to particular store addresses. In particular it contains the page address registers, which are used to map the memory addresses used by programs onto the core or drum store addresses where the data actually resides, under the one-level storage system.

Atlas 2 has a similar register structure, but only core store as main memory – see Figure 3. It also has a slave store and fast operand registers.
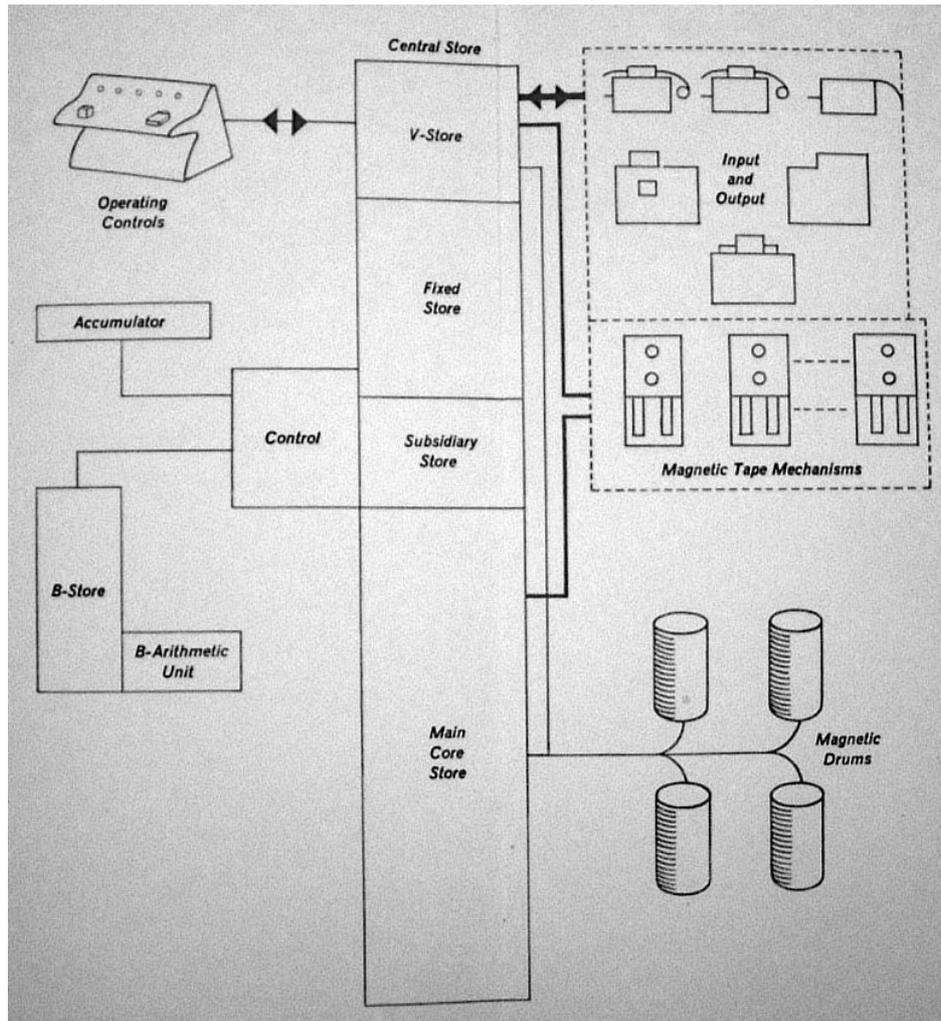
Figure 4: The Structure of Atlas 1

3. System & Configurations

See Figure 4. **Atlas 1** has a minimum main memory of 114,688 48-bit words of which at least 16,384 are in core store and the balance in drums. Each 24-bit half-word has a parity bit. The fixed store has 8,192 words with an access time of 0.3③s and an associated private working store of 1,024 words with an access time of 2③s.

The B store, which contains the 128 index registers, has an access time of 0.35③s, while the main core store has an access time of 2③s, but this is effectively reduced by providing a number of access systems to different areas of the store. Drums have 24,576 words each, an average latency of 6ms and a transfer time for a 512 word block of 2ms. An installation contains typically a minimum of four drums; a cabinet holds 4 drums, so there would normally be a multiple of four in an Atlas 1 installation.

Transfers from all devices, except the drums and Ampex magnetic tape decks (which are used for system purposes), are handled by a single peripheral co-ordinator in the fixed store programs, via single character buffers. The latter vary according to the device – e.g. 7 bits for paper tape, one column for punched cards or 16 bits for IBM-compatible magnetic tape.

Two types of co-ordinator are available. Using the most powerful, the following shows the maximum peripheral configuration:

<u>Type</u>	<u>Number</u>
Ferranti 5-track paper tape reader (300cps)	8
Ferranti 8-track paper tape reader (1000cps)	4
Teletype 110 paper tape punch (110cps)	8
Creed 3000 paper tape punch (300cps)	4
Creed 75 teleprinter	4
Analex 4/1000 line printer (815-1000lpm)	4
ICT593 80-column punched card reader (600cpm)	4
ICT582 card punch (100cpm)	2
Graphical output (4k by 4k array)	1
IBM magnetic tape channel allowing up to 3 decks	1
General 24-bit in/out channel	6
General 12-bit in/out channel	12
General 4-bit in/12-bit out channel	12

Ampex TM2 1" tape decks are separately attached via 8 channels, allowing a maximum of 32 decks to be attached. A switching unit controls 8 decks on two channels, allowing two of each group of 8 decks to operate simultaneously. The tapes are pre-addressed and transfers are in blocks of 512 words with an effective user rate of 64,000cps.

The main console has a paper tape reader and punch and a teleprinter, used by the Supervisor program and the operator to communicate. Slave consoles lack the teleprinter, while an engineers' console also contains the engineers' lights and switches for maintenance. Figure 5 gives the manufacturer's idea of a typical Atlas 1 installation.

Atlas 2 has a peripheral co-ordinator and a magnetic tape co-ordinator (see Figure 3) to which is attached a switching unit. It offers similar peripherals to Atlas 1, and in addition a disc store with a capacity of up to 12 million words and a revolution time of 50ms. 512-word blocks are again used.

A typical Atlas 2 installation is taken to be:

> 32k 5③s core store plus B store, V store, slave store and fast operand registers (the alternative is 2.5③s store)
> 8 Ampex TM2 magnetic tape units
> 1 peripheral co-ordinator
> 3 paper tape readers
> 2 paper tape punches
> 3 teleprinters
> 2 card readers
> 1 card punch
> 1 line printer
> 1 engineers' panel.
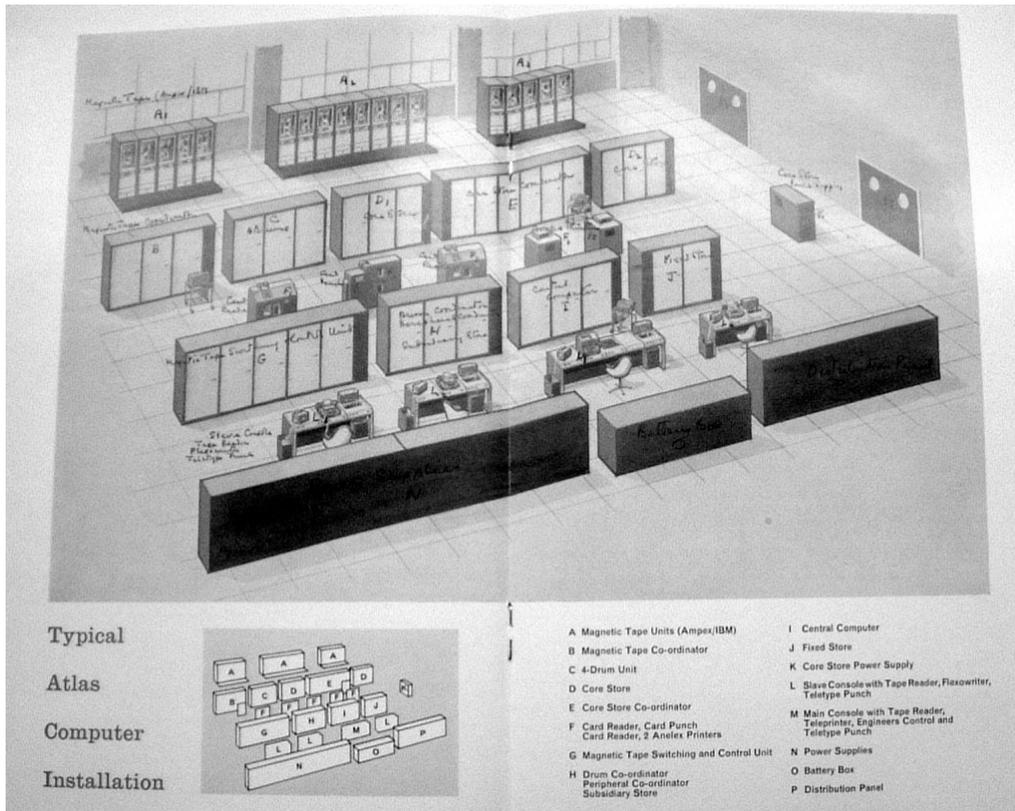
Figure 5: A 'Typical' Atlas 1 Installation

4.   The Operating System

The operating system for Atlas is known as the Supervisor. Much of it resides in the fixed store, but it also occupies main memory, according to its availability from other tasks. The Supervisor is supported by special hardware which allows it to control all activities of the Atlas system including the scheduling of user programs and the operation of all peripheral transfers. The Supervisor is entered automatically in any of the following situations:

a) a piece of peripheral equipment signals that it needs attention
b) a user program obeys an extracode that needs Supervisor attention, e.g. for a peripheral transfer
c) an error occurs, such as division by zero in a user program, or a general system error
d) a predetermined time (or number of instructions obeyed) elapses.

User programs and data are divided into *documents*; these are either a piece of program, some data or a job description. They may be entered in any order on any combination of input devices. The job description lists all other documents required for a particular job and provides the Supervisor with estimated requirements for scheduling purposes. The scheduling functions of the Supervisor are illustrated in Figure 6. The input supervisor assembles documents into the input by Supervisor decision. In a similar way, output from user programs is spooled into a magnetic tape based output well, whence it is sent to the output peripherals selected by the programmer. Input documents are "line-reconstructed", e.g. from paper tape input delete characters are removed and backspaces are interpreted in the same way that a printer would.
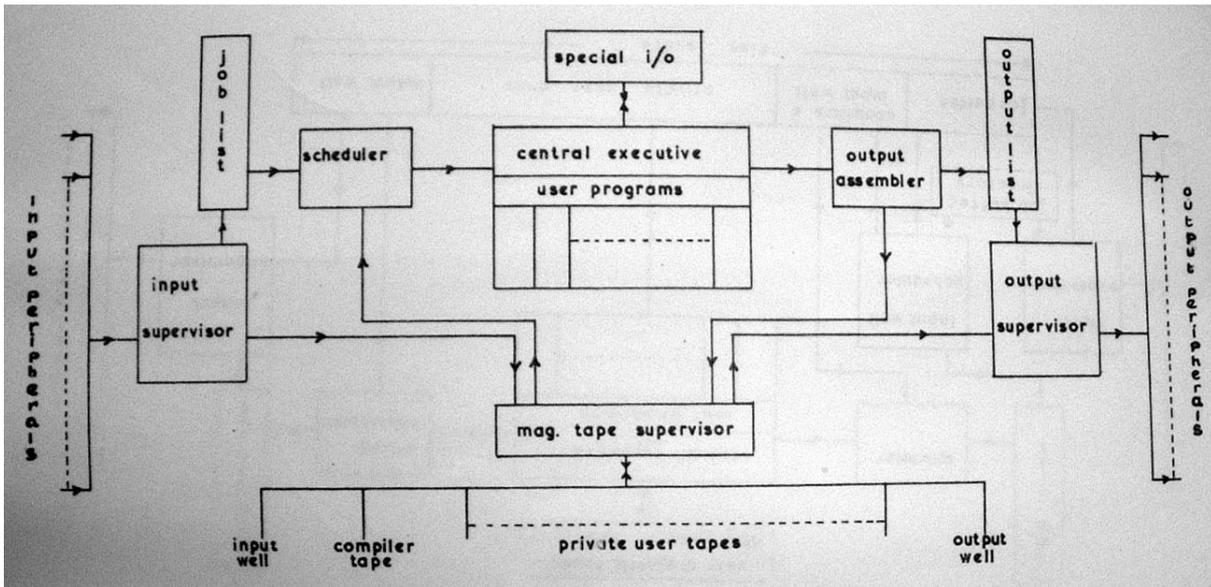
Figure 6: Supervisor Scheduling

Each user program uses memory addresses starting at zero, but the actual addresses assigned to it will depend on where it is allocated space by the Supervisor. When a program is loaded it is allocated a number of 512-word blocks and hardware maps the addresses used by the programmer on to the actual addresses automatically. It also prohibits access outside the area that has been allocated, thus protecting the Supervisor and other user programs from interference. In addition, on Atlas 1 (but not Atlas 2), these blocks may be moved between core and disc storage as needed, thus creating the one-level store.

5. References

The following references in section **X5** are most relevant to this section:

1, 8, 10, 14, 16, 20.