Systems architecture

The Orion system was conceived and launched in 1958 . This was the first design of a system which used ballot box logic based on magnetic principles in the form of circuit packages called 'neurons' proposed by Gordon Scarrott then Ferranti's Chief Engineer. These were to be the basis of the ORION mid range computer running at a clock of 500 kiloHerz. machine walls particularly aimed at data processing users but was also intended to satisfy the needs less demanding scientific users needing a lower cost general-purpose computer with less capability than the Mercury and later Atlas top end scientific computers which were developed in conjunction with Manchester University. Furthermore Orion was to be a Ferranti 'own brand' computer following the successful Pegasus 2 and Perseus machines aimed at the data processing market. Indeed Orion was to use and did use a Pegasus derived and enhanced order code. Later this became the ORION 1 system.

In the event development of the totally new ballot box logic took some 5 years which meant that deliveries were very late. Notably an order from Prudential Assurance Company was put at risk and Peter Hall the manager of the computer department authorised construction of the ORION 2 computer which would be logically similar but use proven circuitry and run at twice the ORION 1 speed in order to retain this order. Orion 2 was authorised in September 1961 and delivered on time to its first customer in September 1964. It was based on developed versions on the so-called 1959 'Gribblon' circuits which by that time had become well known in North America as DTL logic complemented by UK designed circuits needed only by Orion 2 such as cable drivers. .

Word length was 48 bits of which 7 bits are function bits. Register structure is given as a diagram elsewhere in this profile. The function of the various registers of Orion systems has been given by Ted Braunholtz the innovator of the Orion system at a logical level as follows :

A, B, C	The main registers for the data. Multiplicand in A, double length product in B & C.
D	Used in division and access to all the cable driver circuits when so programmed.
E	Counts number of iterations in multiply, divide and shift.
F, X, Y, Z	the instruction
J	the instruction address
W	if there are a sequence of pre-modify instructions this marks where the instruction started.
U, V, T	believed to be allocated by programmers as required.

In addition to the above hardware registers there are a number of pseudo registers in core store which can be used for specific purposes.