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EMIDEC 2400 Systems Architecture.

1. Background and project origins.

Precise information on the origins and dates of the EMIDEC 2400 project has not yet come to light. The ex-EMI engineer Ron Claydon says (ref. 1) that the team developing this computer "was led by Charles Kramskoy and included Norman Brown and Bill Talbot. Later I took control of this project, while Charles Kramskoy became EMI Electronics Chief Engineer. Around the same time, Norman Hill joined us from Elliotts as Sales Manager for computers: he was responsible for the sales of nearly all the Emidec 1100s and 2400s.

John Hendry (ref. 2) says that Hill joined EMI early in 1957. Hendry, a commentator on the history of technology writing thirty years after the events, states that "in the summer of 1955 Kramskoy, then at EMI's Special Products Group at Feltham, put a proposal to the National Research Development Corporation (NRDC) for a computer based on core-plus-transistor logic and magnetic tapes. Work was under way early in 1956 on what was by this time called the 2400". However, the computer that finally emerged had transistor-diode logic – (it was the EMIDEC 1100 that had core-plus-transistor circuitry). Clayden's evidence suggests that Hendry's dates may be one year too premature.

Hendry goes on to say that "from mid-1957 the 2400 was treated as a one-of-a-kind high-tech R&D project, progressing concurrently with (but independently from) the [EMIDEC] 1100 project". Hendry says that the EMIDEC 2400 'was first working' in 1961.

Campbell-Kelly says (ref. 3) that "the EMI 2400 had been developed under the auspices of Lord Halsbury and the NRDC, and was intended to be Britain's answer to the IBM 7090 large-scale EDP computer. This it would have been, had it not had profound reliability and software problems ... In the event, only three EMI 2400's were ever sold".

Reviewing all this evidence, the best guess is that the EMIDEC 2400 project started in the autumn of 1957 and finished in the spring of 1962. The date of the first delivery to the Ministry of Pensions is not known, though Campbell-Kelly says that this occurred in 1961 at a price of about £500,000 (ref. 3). The computer interests of EMI were absorbed by ICT in July 1962 and the EMIDEC 2400 development was soon abandoned.

2. System overview.

The following notes are taken from refs. (4 and 5). The EMIDEC 2400 is a 36-bit word, binary computer having parallel data highways. The computational circuits are based on transistor-diode logic operating at a clock rate of 1MHz. Typical logic switching times are approximately

200 nanoseconds and the parallel adder is asynchronous. Main RAM consists of ferrite core storage. There is a fast cache made from diodes and capacitors.

Great emphasis is based on the use of magnetic tape as secondary storage, particularly since the EMIDEC 2400 is targeted at the business data processing market. There are two types of system: one-inch wide tapes with fast start/stop times; four-inch wide tapes with slower start/stop times. Business data-processing applications are further catered for by the provision of alphanumeric character-handling facilities and hardware instructions for conversion between binary and either decimal or sterling.

3. The Central Data Processor (CDP) and main memory.

The CDP uses 36-bit words (plus one parity bit). 6-bit characters are employed. Multi-words are catered for – see later. The CDP contains a 36-bit parallel asynchronous adder with an average add-time of 0.6 microseconds. Plug-in printed-circuit boards measuring 7 inches by 3.5 inches are mounted in racks measuring 6 feet high by 3 feet wide by 2 feet deep. A number of racks are bolted together to form the sub-units of the complete computer.

The main (primary) memory is 4K words of magnetic core storage, extendable to 8K words, with a 15 microsecond cycle time and 6 microsecond read time. Each word of core storage is of 37 bits: 36 data plus one parity bit. There is a fast 64-word cache of diode-capacitor storage having a cycle time of 4 microseconds and a read time of 1.5 microseconds. Cache words may be used as general-purpose registers, as address-modification registers (B-lines), for input/output control or for storing small program loops. Each word of the diode-capacitor store is of 38 bits, the 38th bit being used as an independent, program-accessible, switch. (See section M2/X3 for the EMIDEC 2400's full instruction set).

Instructions are held either in core memory or in the fast 64-word cache. Block transfers (of up to 15 words) may be made between these two stores. The results of multiplication and division are placed in the cache. The CDP runs a *Master Control Program*, capable of handling a number of concurrently-active tasks.

The fundamental 36-bit unit of information in the EMIDEC 2400 is called a *brick.* This can be used either for conventional binary data or for variable-length alphanumeric quantities. When used as binary data, one bit specifies *binary* and the remaining 35 bits hold a value in two's complement form. For alphanumeric strings of up to 15 bricks in length, the first (most-significant) character of the first brick identifies the alphanumeric format and gives the number of bricks in the string. The alphanumeric coding provides for the 26 letters of the alphabet, the numerals 0 to 11 and some special control characters. Both binary and alphanumeric data can be stored on magnetic tape. A record can be any desired number of words in length. The block length can be varied to suit an application.

The CDP has up to four I/O buffers, each with two 36-bit words of diode-capacitor storage. These buffers are used to interface I/O equipment (including the magnetic tape decks) to the CDP and are similar to the *channels* employed by other contemporary computer manufacturers. The I/O buffers provide for autonomous input/output transfers.

Interrupt-handling. When one of the events listed below occurs, a return-link is stored, information giving the type and cause of interruption is placed in a pre-defined location in memory and an interrupt routine is automatically entered. The recognised causes of interruption are as follows:

Primary memory parity error.
Buffer parity error.
Divide-by-zero.
Buffer has detected a control word on magnetic tape.
Peripheral equipment interrupts, due to one of the following reasons:
- Power failure or excessive rate of data errors;
- Parity errors on four-inch tape system;
- Single data-errors (corrected) and double errors on one-inch tape system;
- Peripheral device in a controlled stop state;
- Program Interrupt switch pressed on the operators console.

4. Magnetic tape system.

The one-inch systems have the following properties:

Transfer rate: 20Kcharacters/sec., single error-correction.
Two channels per tape deck; 12 tracks (6 data, 4 check, 2 timing) per channel.
Packing density: 100 bits/inch longitudinally
Transport speed: 200 inches/sec.
Start or stop time: less than 5 milliseconds.
Each reel of one-inch tape is 2,400 feet long.

In the EMIDEC 2400 system there is a common bank of up to about 20 one-inch magnetic tape decks, each being switchable between a number of (independent) processing units. One of these processing units is the mandatory *Central Data Processor, CDP*. From perusal of the available original documentation, it is believed that to this may be added a number of other so-called *Peripheral Units.* These are basically small special-purpose computers each having its own built-in (fixed) program.

The four-inch magnetic tape systems (also called *Data File tapes*) have the following properties:

Transfer rate: 20Kcharacters/sec.
10 channels per tape deck; 9 tracks (6 data, 1 check, 2 timing) per channel.
Packing density: 100 bits/inch longitudinally
Transport speed: 200 inches/sec.
Reversal time: 3 seconds.
Each reel of four-inch tape is 2,400 feet long.

The switching of tape decks is either controlled manually from an operator's control desk or by software via the *Master Program*. For the latter, a hardware *Switching Unit* is able to switch tape decks automatically between the Central Data Processor's buffers and the Peripheral Units, with interlocks that ensure that 'busy' units are not switched mid-way

through transfers. Variable-length block transfers may be accompanied by gather-scatter facilities.

EMI magnetic tape formats allow special control and locational (block-addressing) markers to be written to tape. These markers can be processed within the tape drive, thus avoiding CDP activity. A special CDP instruction, known as the *Console Order*, enables software to:

(a) connect or disconnect magnetic tape units from the Peripheral Units;
(b) signal to Peripheral Units, requesting that their current process be terminated;
(c) transfer Peripheral Units and tape decks to manual control;
(d) indicate to the operators when changes are necessary to tape reels;
(e) display messages at the central console to indicate special operator-action or status-information.

5. Peripheral Units for off-line data entry, etc.

An EMIDEC 2400 system supports four types of peripheral data-processing activity that can proceed relatively independently of the CDP. These are believed to include:

(a). A special stand-alone **input unit,** which allows up to 112 keyboards to input data to a magnetic tape deck in off-line mode. Some data-checking facilities are incorporated.

(b). A stand-alone **output unit,** which accepts data from magnetic tape and feeds this to a lineprinter or to a card punch.

(c). A stand-alone **card/tape converter,** which accepts data from either cards or paper tape (5 or 7 hole) and writes this to magnetic tape in standard EMIDEC 2400 format. The unit will also punch cards from data held on magnetic tape. Two-way conversion can take place simultaneously if required. The data-rate from paper tape is 300 characters/sec. and from cards is 300 cards per minute. Cards are punched at 100 cards per minute.

(d) A **File Search Unit,** which contains a small dedicated processor to which is attached magnetic tape decks. One of these contains a ‘control’ tape; another contains a ‘results’ tape. The File Search Unit searches data on a four-inch tape as determined by the control tape, returning matches to the results tape. The search rate is about 15 Kcharacters per second.

6. References.

1. Ron Claydon, Early Computer Developments at EMI. Resurrection (the bulletin of the Computer Conservation Society), Number 16, Christmas 1996.

2. John Hendry, *Innovating for Failure: government policy and the early British computer industry.* MIT Press, 1990. ISBN: 0-262-08187-3.

3. M Campbell-Kelly, *ICL: a business and technical history.* Oxford University Press, 1989. ISBN: 0-19-853918-5.

4. Emidec 2400 Data Processing System: general description. Undated 8-page brochure issued by EMI Electronics Ltd. Computer Division, Hayes, Middlesex. (Printer's reference code: ES17/1064/5M/360/BP).

5. Emidec 2400 Data Processing System: technical specification. Undated 10-page brochure issued by EMI Electronics Ltd. Computer Division, Hayes, Middlesex. See: http://www.vintage-icl-computers.com/icl44aaa