Version 2, November 2011 **E6X2**

Systems architectures for the Elliott 4100 Series computers.

The specification and hardware design for the Elliott 4100 series had largely been completed by 1964. There were two members of the 4100 series family, of which the 4120 was the first to be delivered to an outside customer in 1965. The more powerful Elliott 4130 computer came next, with the first delivery being in 1966. When Elliott-Automation's main computing interests were absorbed into ICL at the end of 1968, the 4100 series were the only Elliott computers to be marketed by ICL. The manufacture of the 4100 series ceased in about 1970.

The 4100 series machines were based on bit-parallel CPUs employing silicon transistors. For each of the 4120 and 4130 computers there was originally a choice of ferrite core store: either 2 microsecond or 6 microsecond cycle time. The 4130 had a faster CPU and implemented floating-point operations in hardware. Floating-point was performed by software extracodes in the 4120. The Autonomous Transfer Unit (ATU) was an add-on extra for the 4120 but was built into the main cabinet of a 4130.

	4120	***4130***
Word length, bits	24	24
Number of instructions per word	1 or 2	1 or 2
Max. installed memory at 2 microseconds (µsec.) cycle time	64K words	256K words
Fxpt ADD time, direct addressing mode, with 6 µsec. store	12.0 µsec	12.0 µsec
Fxpt ADD time, direct addressing mode, with 2 µsec. store	5.6 µsec	4.5 µsec
Fxpt MPY time, direct addressing mode, with 6 µsec. store	67.0 µsec	22.0 µsec
Fxpt MPY time, direct addressing mode, with 2 µsec. store	60.6 µsec	15.0 µsec
Floating-point hardware?	No	Yes
Flpt ADD time, direct addressing mode, with 2 µsec. store	199 µsec.	15 µsec.

Table 1. Overall characteristics of Elliott 4100 series computers.

The physical dimensions of a basic Elliott 4130 processor were: height 63.5 inches (161 cms), width 70 inches (178 cms), depth 26 inches (68.5 cms), weight 1040 lbs (450 kg), power consumption 2 kVA.

The Elliott 4100 series' 24-bit word employed two's complement representation for integers. Single-address format instructions were either short (12 bits) or long (24 bits). A long instruction may be split across two consecutive memory locations, in which case the instruction takes a little longer to execute. The program counter, S, refers to the half-word address of the next instruction. The effect of obeying an instruction in the second half of a word which has just been altered by the instruction in the first half of the same word is not defined. For many applications, four six-bit characters were stored per word. When held in

memory, floating-point numbers were normally rounded and packed into two words containing 39 bits of mantissa and 9 bits of exponent.

As is described in section E6/X3, the Elliott 4100 series had a comparatively powerful repertoire of addressing modes. The series also implemented a neat and comprehensive mechanism for handling the various condition-bits (eg accumulator sign, overflow, interrupt, etc.) that contribute to the current status of a computer. The concept of a stack, as used for example in block-structured languages, is given hardware support – see the MVE and MVB instructions given in section E6/X3. There was hardware assistance for packing and unpacking characters. A distinction was made between the three forms of shift, namely *logical*, *arithmetic* or *circular*. There was a flexible set of instructions for register-to-register moves. Finally, the Elliott 4100 series had a Standard Interface for all input/output devices, the physical manifestation of which was a pre-defined plug and socket arrangement for all peripherals. The Standard Interface has eight *data-in* lines, 8 *data-out* lines, three interrupt lines and eleven other control, status and timing signals.

The Elliott 4100 has the following programmer-accessible registers. When describing digit-positions, the 4100 convention is that bit 24 is the left-hand (most-significant) position and bit 1 is the least-significant position.

	size, bits	***description***
M	24	main accumulator
R	24	reserve accumulator, also used as the address-modification register, etc.
S	17	program-counter, also known as the sequence-control register
K	12	count register
C	14	conditions register, of which bits 16 – 7 are unallocated.

Programmers also used the following abbreviations for the (software) quantities shown:

I	Normal Interrupt word (12 bits)
A	Attention Interrupt word (12 bits)
FPA	Floating point accumulator (39-bit mantissa, 9-bit exponent)
DPA	Double length floating point accumulator (87-bit mantissa, 9-bit exponent)
CPA	Complex floating point accumulator.

A wide range of peripheral equipment was available for the Elliott 4100 computers, including magnetic tape units, exchangeable disc units, graphical output devices and plotters.

Elliotts were well-regarded for their graphical displays in the mid-1960s. The type 4280 Graphical Display Unit had a 10 inch by 10 inch viewing area with 1,024 x 1,024 addressable positions, giving a resolution to within 0.01 of an inch. The image was automatically re-generated ten times per second from a display file held in the computer's main memory, to give a flicker-free picture. Curves or lines could be drawn at the rate of 100 microseconds per displayed inch. The type 4280 unit included a vector generator for drawing straight lines, a character generator which displayed the alphanumeric characters of the 4100 series internal codes in three sizes (5/64th inch, 5/32nd inch or 5/16th inch) and

a hand-held *light pen* which enabled the user to identify points on the display. (The light pen achieved the same effect as a modern mouse and cursor).

The disc equipment offered for the Elliott 4100 series computers in 1967 consisted of ten disc surfaces, each with 100 tracks split into 16 sectors of 64 words. The on-line capacity was therefore about one million words. The read-write heads took about 100 milliseconds to traverse 33 tracks and, once the desired *cylinder* of tracks had been reached, the mean access time was 12.5 milliseconds and a sector could be transferred in 1.5 milliseconds.