Version 2, November 2011 **E5X2**

Systems architecture for the Elliott 900 series computers.

Note: all references are listed in section E5/X5.

General overview of the family.

The 900 series of computers, which first appeared in 1961, lasted in one form or another until the mid-1980s and sold in their thousands. Originating from Elliott's efforts to meet the Army's need for 'mobile computing' for artillery control, most of the 900 series derivatives came to be used for aerospace applications – though civil and industrial variants were also successfully produced.

Starting with an 18-bit word length, 13-bit and 12-bit variants were to appear later. The 900 family of parallel (ie not bit-serial) computers spanned technologies ranging from discrete transisitors to integrated circuits, and from ferrite core memory to semiconductor memory. By the end of the 1970s several of the early commercial users had passed their 900 series computers on to schools and colleges, where they operated happily for some years.

An enthusiastic Elliott company brochure (reference 32), written in 1967/68 and half way through the 900 series' design life, tells the family's story as follows:

"All the computers in the 900 range are functionally compatible with each other". Actually, this was not strictly true in the end. All the 18-bit word members of the family (see Table 1 below) had instruction-set compatibility; similarly for all the 12-bit word members (see Table 2 below). However, the 12-bit and 18-bit instruction sets differed, as shown in section E5/X3. There was a single 13-bit variant, the ARCH 102 system.

The brochure continues: "The series was introduced by the 920A computer, which is in service with the Royal Navy, the Army and the Royal Air Force". Again, this is not strictly true because there was a 901 experimental computer, designed for an Army tank project, but only one 901 was built. The 920 is described in reference 33.

The brochure continues enthusiastically: "The 920B followed the 920A and with it the first big reduction in cost was achieved. The civil version of the 920B, the 903, is the successor in the title to the highly successful Elliott 803 ... The rapid development of microelectronics … has led to the design of the 920M… Already an even faster yet equally rugged computer is in production: the 920C, eight times faster than the 920B, which is itself two or three times faster than the 920A. Close on the heels of the 920C have come simplified, lower cost derivatives offering the same high performance capacity over a less extreme temperature range. These are the 902 and the 905, and their 'ARCH' equivalents, assembled from a range of rack-mounting units to form highly competitive computer systems for commercial and industrial applications. [ARCH stands for Articulated Control Hierarchy, originally conceived as a modular system of standard

analogue and digital sub-units sharing a common bus]. Newest of all is the microminiature 102C, functionally similar to the 902 but even further scaled down in size to suit military (air, sea and land) mobile installations".

Trying to arrange the family of 900 series computers in chronological order is difficult because: (a) the type-numbering is confusing, (b) there is a scarcity of surviving source-documents, and (c) computer developments proceeded simultaneously in more than one Division of the Elliott-Automation company. Here is an approximate chronological sequence:

Year	***900-series computers introduced in that year***
1961	901
1962	920A
1963	920B,
1964	ARCH 102
1965	903, ARCH 9000
1967	920M, 920C,
1968	902, 905, 102C/Minim, ARCH105, ARCH 9050
1973	12/12
1976	920ATC, 920 AT
1977	MC1800.

Elliott's Mobile Computing Division played a significant part in the early development of the 900 series. Thus, the initials *MCS* were often used in the marketing name of 900 series machines. Examples are: MCS 900, MCS920, MCS920B, MCS920C. Further aliases occurred. For example, an Elliott MCM2 computer was a MCS 290M with 8K words of 5 microsecond core memory reference 34.

By 1970 much of the 900-series design emphasis had moved from Borehamwood to Rochester where the 920 ATC and the 12 /12 Series were to provide the basis of all of GEC/Marconi's airborne computer developments until the mid-1980s. By then, not all Rochester's innovations were downwards-compatible with the original 900-series family. For example, the 12/12 computer was designed to have a 12-bit instruction word and also, as far as possible, the same instruction set throughout all the different variants of the machine (reference 35). However, different length operands were devised to suit different aerospace applications.

The 18-bit members of the 900 series.

The 920A. The Elliott 920A, originally called the MCS920 or simply the 920, was the first full production member of the range. Its instruction set was similar to that which soon became the standard 900, as listed in section E5/X3, except for minor differences in functions 8, 11, no block transfers and only 7-track (not 8-track) paper tape input (references 2, 36).

The first 920 system, retrospectively called the 920A**,** had much slower multiplication and division than subsequent family members. It also offered very limited options for primary memory, namely: (a) 4K words at 6 microseconds cycle-time, or (b) 8K words at 8 microseconds cycle time. The program counter, known as SCR or later simply as S, and

the B (modifier) register were actually held in main memory. Thus, the instruction times included the need to access SCR, as well as fetching the instruction and any operand-fetching. Accessing and incrementing SCR (the program counter) took 9 or 11 microseconds (4K or 8K store). The sample 920A instruction times quoted below are without address-modification. If modification was called for, then 6 or 8 microseconds should be added to the times:

Function	***time with 4K 6µ memory***	***time with 8K 8µ memory***
Add	21 microsecs.	27 microsecs.
Multiply	183 micrrosec.	189 microsecs.

No extensions to the basic memory capacity were offered. The 920A was packaged in a box measuring 36 x 12 x 14 inches (military) or 34 x 10 x 33 (civil), and weighing 170 lbs (78 kg) military or 80 lbs (36 kg) civil. The July 1964 prices for the 920A (reference 37) varied between £21,300 and £26,500, depending upon the choice of memory and packaging options. The power supply unit was extra, typically £750. A complete 920 system with paper tape reader, punch and flexowriter might typically cost £31,534.

The other 18-bit members of the Elliott 900 family.

The more popular, and compatible, 18-bit 900-series computers are listed in Table 1, for which the information comes mainly from the Elliott FACTS booklets for each machine.

	903	***905***	***920B***	***920M***	***920C***	***920ATC; MC1800***
Primary memory, standard.	8K	8K	8K	8K	8K	16K for ATC
Memory cycle-time options, microseconds.	6	1 or 2	6	2 or 5	1	1 for ATC
Max. addressable memory	64K	128K	64K	32K	128K	?
Includes an H register?	no	yes	no	no	yes	?
Add time, microsecs., unmodified	23.5	2.4 or 4.4	23.5	10.6 or 19	2.2	2.2
Multiply time, microsecs., unmodified	76.5	10.2 or 12.2	76.5	29.6 or 38	9.0	9.0
Basic package, measurements in inches or cubic feet. *Note: ATR = Air Transport Racking.*	Desk, 43 x 26 x 37	Desk, 42 x 24 x 36, or rack-mounted	Military pack, 19 x 9 x 32	Military pack, 12.56 x 7.5 x 7.63	Military pack, 0.5 -> 1 cu. ft.	Military (1 ATR short, incl. power supply

Table 1: Overall characteristics of some of the 18-bit members of the Elliott 900 family.

The instruction times in Table 1 are for unmodified addresses. Modified instructions are naturally slower. For example, the unmodified/modified times for the 920M are: add =

10.6/13.8 microseconds; multiply = 29.6/32.8 microseconds. The process of modification is not allowed to change the F bits in a 900-series instruction (unlike the effect of modification in the case of the earlier Elliott 400 and 800 series computers).

The memory cycle times in Table 1 are nominal. Minor alterations occurred over the life of each type of machine. For example, in October 1969 an engineer's data sheet specified the following options for a 905:

MC5/13: 16K words at 1.8 microseconds
MC5/12: 16K words at 1.2 microseconds
MC/15: 8K words at 1.0 microseconds.

Elliott sales and marketing terminology provides another source of potential confusion for the computer historian. For example, an Elliott MCM2 computer was a 920M with 8K of 5 microsecond memory.

As an example of the type of hardware employed in one of the machines in Table 1, the CPU of a 920B/903 contains 75 circuit boards, measuring 8″x5″ (20x13cm). Most of these are populated with *Logic Sub-Assemblies*, typically 14 to a board. Each LSA can hold up to three transistors plus other components, and so can implement up to three conventional logic functions using Diode-Transistor Logic. For example, LSA01 implements three 2-input NAND gates, LSA03 is a 4-input NAND gate and two NOT inverters.

As another example, the 920M is constructed from about 450 relatively inexpensive integrated-circuit modules and includes a miniature 8192-word core store, all housed in three hinged segments, two containing logic and the other the store and its circuitry. When closed up, the 920M measures only 12.56″ x 7.50″ x 7.63″ [30.8 x 18.4 x 18.7 cm]. This three-layer configuration in the form of an ATR package is very suitable for the computer's aerospace applications.

Other family members compatible with the machines shown in Table 1 are now briefly described. The 18-bit ARCH 9000 process-control variant has a similar performance to the 903 and 920B. The 18-bit ARCH 9050 has a similar performance to the 920C and 905. The software-compatible 920ATC and the MC1800 were both 18-bit computers developed during the 1970s specifically for airborne applications. The 920 ATC (Advanced Technology Computer) was developed for aerospace applications at Rochester and was the first 920-derivative to have floating-point hardware. The 920 ATC performed its flight trials in 1976/77 and went into production in mid-1977.

The MC1800 was produced in the mid-1970s by Marconi Space and Defence Systems which, like Elliott Brothers (London) Ltd., became part of the GEC empire in 1968. Quoting from reference 30, the MC1800 is described as a new product: "born out of experience gained from the internationally proven 900 series … the MC1800 has been microprogrammed to emulate the 920C to provide compatibility with computers already in service with the Royal Artillery and Field Artillery Computing Equipment (FACE) and the Royal Air Force Jaguar and Nimrod aircraft…. The CPU design is based upon the AMD 2901 bipolar, bit-sliced microprocessor…. The standard CPU accommodates up to 2K of 48-bit words of EPROM of which the 920C emulator occupies approximately 0.5K words". Several main memory options are available. The CPU interfaces directly to 16K and 32K modules. A 64K module is also available. The MC1800's word length is 18 bits and

addressing is up to 128K (using the H register). The add-time is 2.1 microseconds and the multiply time is 9.9 microseconds. These 1979 speed figures are marginally slower than those quoted in the earlier 1977 edition of the brochure (reference 30), indicating that the MC1800 probably did not go into production until perhaps 1978.

The 18-bit instruction format for all the computers featured in Table A6.1 was as follows:

1	4	13
B	**F**	**N**
Modify	Op code	address

The 12-bit word members of the 900 series family.
These computers, sometimes referred to as the *cut-down* members of the 900 series, necessarily performed arithmetic to 12-bit, rather than 18-bit, precision. They also had a more limited addressing capability, a more cumbersome method for achieving address-modification and a reduced number of priority levels. The main 12-bit family members are shown in Table 2.

	902	**102C (or Minim)**	**ARCH 105**	**12/12**
Primary memory, standard.	4K	4K	4K	*(see text)*
Memory cycle-time options, microseconds.	1 or 2	1 or 2	1 or 2	*(see text)*
Max. addressable memory	32K	32K	32K	*(see text)*
Add time, microsecs	2.4 or 4.4	2.4 or 4.4	2.4 or 4.4	*(see text)*
Multiply time, microsecs	11.4 or 13.4	11.4 or 13.4	11.4 or 13.4	*(see text)*
Basic package, measurements in inches.	Cabinet, 19 x 42 x 23 (rack-mounted)	Military pack, 5 x 19.63 X 7.63	Twin bays, each 23 x 24 x 41	*(see text)*

Table 2: Overall characteristics of the 12-bit members of the Elliott 900 family.

The Elliott 102C was at the heart of the Minim Navigation Management System produced by Elliott Flight Automation Ltd., Airborne Computing Division, in approximately 1968 – see references 38, 39. Hence, the name *Minim* is sometimes used to denote the 102C computer.

The 102C was designed from the start for airborne use, to environmental standard DEF 133 class A, which includes an impressive operating temperature range of - 40˚ C to + 85˚ C. The 102C's case conforms to ATR (Air Transport Racking) ARINC standard for ½ long ATR.

The 12/12 airborne computers started off by being generally compatible with the 12-bit Elliott 900 family, though reference 35 states that: "the flexibility can be taken further by

extending the data word length to 24 bits". The earlier versions of the 12/12 had a 2 microsecond cycle time, 4K memory.

The Elliott 12/12 came in at an exciting time in airborne computing when the traditionally analogue field of *flight control* (aerodynamic stability, engine control, etc.) was beginning to be influenced by the digital successes in the field of *mission systems* (navigation, weapons-aiming, etc.). By 1972, airborne analogue computing was poised to go digital. The 12/12P was probably the first production version to be introduced, in 1973. It had a 4K, 2 microsecond, core memory and instruction times very similar to those quoted for the Elliott 102C/Minim in Table 2 above.

The 12-bit instruction format for all the computers featured in Table A2 is as follows:

4	1	7
F	**M**	**N**
Op code	Mode	Operand addr.

The registers for the 12-bit members of the Elliott 900 family are as follows:

S register (program counter): 13 bits, extensible to 15 for a 32K store;
A register (accumulator): 12 bits;
E register (accumulator extension): 11 bits;
B register (modifier): 12 bits;
D register (pointer): 6 bits, extensible to 8 bits.

D is used with the seven N bits to make a total of 13 (extendable to 15) address bits and in the original documentation V is used to signify [N extended by D].