Version 2, November 2011 **E4X2**

Systems architecture for the Elliott 502 computer.

Note: all references are listed in section E4/X5.

The prototype 502 used germanium transistors but the later machines were believed to have been a redesign using silicon transistors which had by then become available (reference 1).

Apart from using a somewhat similar general form of exterior cabinet construction, the Elliott 502 had no connection with the Elliott 503 computer which was the more powerful version of the Elliott 803 – (see section E3). Furthermore, the latter stages of commissioning the 502 took place at Rochester, rather than at Borehamwood, because the special purpose equipment to interface the 502 to the RRE radar system was being developed at Elliott's Rochester factory. The cost of each Elliott 502 computer is not known but, by comparison with the known figures for an Elliott 503, it is estimated that each Elliott 502 probably cost between £250,000 and £450,000 (1965 prices).

The Elliott 502 was a high-performance parallel, transistorised computer. It was described as *asynchronous* (reference 2, and see below) and as incorporating "the application of ultra-high-speed techniques to systems in which the time allowed for computing is the actual duration of the related event", resulting in "making a spectacular increase in the range of systems to which automatic on-line data processing can now be introduced" (reference 3).

The central processor was indeed asynchronous, in the sense of there being no fixed-frequency clock. This was a first for Borehamwood. Iann Barron, who worked on the Elliott 502, describes the asynchronous nature of the computer as follows (reference (4): "There was a central timing system consisting of a chain of delays, which emitted the timing signals for a cycle; the length of the delay was preset (adjustable), but the number of delays (and sequence) of delays was variable, depending on the operation that was occurring, so there was no fixed clock period. The completion of a sub operation was timed by fixed delay appropriate to that sub operation, and not by a completion signal generated by the logic of the sub-operation (I am not sure that was true for an arithmetic carry operation)". The use of a chain of delays was also employed in the asynchronous Atlas computer (reference 5), where the delay-chain was known as the *Juke Box.*

The 502 had two sections of ferrite core memory: a fast section of 1K 20-bit words (approximately equivalent to 2.5K bytes) and a main section extensible 'up to any practical limit' in units of 8K words. The cycle-time of the fast section is 1.25 microseconds and that of the main section is 3 microseconds. Programs may be obeyed from either store, and operate on data from either store. Input/Output is either via Direct Transfer or via Autonomous Data Transfer. Autonomous data transfers to/from peripheral devices only take place to/from the main section. Provision is made for a maximum of 12 peripheral devices to have independent autonomous data transfer facilities, any simultaneous requests being handled on a priority basis.

A feature of the Elliott 502 is that it allows the apparently-simultaneous running of several programs on a time-division basis, according to pre-assigned priorities. Up to eight levels of priority are catered for. A system of interrupts (also called *External Stimuli* or *Programme Stimuli*) allows *Program Breaks*, which enable a high priority program to take precedence over one of lower priority in response to an external event. Seven of the priority levels are associated with external interrupt signals; the eighth level is the default level, applying when no interrupt has been received.

The 502 consists physically of five (double-door?) cabinets (reference 3), the construction allowing the whole assembly to be mounted in a trailer for both transportation and operational use. The suite of five cabinets measures 18 ft. long by 2ft 5ins. deep by 5ft 9ins high (5.5 x 0.7 x 1.75 metres), the total weight being 16cwt (813 kg). Cooling is via chilled air, employing a separate refrigeration unit. Besides the connections to/from the equipment being controlled and any necessary autonomous data transfers (described below), the 502 has provision for magnetic tape decks and for the following standard input/output equipment: 5-track paper tape reader, transferring at 500 characters/sec.; 5-track paper tape punch, operating at a maximum speed of 100 characters/sec. In addition, Creed type 75 Keyboard teleprinter and transmitter equipment is provided for off-line working.

According to reference 6**,** a real-time applications compiler, BASIC CORAL, was working for the Elliott 502 computer from November 1966. The system software details are given in reference 7**.**

Systems architecture and visible registers.

In the Elliott 502, fixed-point numbers of 20 bits are stored as two's complement fractions. Both single-length and double-length fixed-point multiplication and division is provided. There is no floating-point hardware. There is, however, a hardware square root function. The 20-bit instruction format (see section E4/X3) is of a conventional one-address type, which includes six function bits and 10 operand-address bits.

The central registers included a 20-bit main accumulator (A), a 20-bit auxiliary, or extension, accumulator (R), a 20-bit modifier register (B), a Sequence Control Register or Program Counter (S), a single-bit overflow register (OV) and a Program Control Register (PCR) which contained seven bits, one corresponding to each Interrupt signal or *Program Stimulus*. The function of these seven bits was to enable, or mask, the effect of the corresponding stimulus. The PCR may also have contained other read-only bits providing the states of the stimuli and the current operating priority level, according to Peter Lawrence who worked on the Elliott 502. The Sequence Control Register, S, contains an extra bit that indicates whether the next instruction is to be fetched from fast RAM or from main RAM.

After obeying each instruction, except for those which have the L (lock) bit set (see section E5/X3), there is a check on whether the highest priority level for which both the external stimulus and the PCR bit are set is the same as the current operating priority level. If not the same, then a *Program Break* operation is performed which:

- stores the current 20-bit working register values, namely S, A, R and B, in memory locations predefined for the current operating priority level;
- sets the operating priority level to that indicated by the stimulus and PCR states;

- sets working register values from those stored in locations defined for the new priority level.

Program operation then resumes, as controlled by these new register values. Note that a program can effectively interrupt itself by setting a PCR bit and so unmasking a stimulus already asserted. The *Program Break* operation, more usually referred to as an automatic context-switch, is comparatively very rapid, taking place in under 10 microseconds.

The Elliott 502's data-paths for input and output are interestingly wide. Direct Transfers take place via a 20-bit bi-directional highway; Autonomous Data Transfers take place via a 40-bit bi-directional highway. More details are given in section E5/X3.