Version 3, November 2011 **E3X3**

Instruction sets and instruction times for the Elliott 800 series and 503 computers.

Note: all references are listed in section E3/X5.

Instruction sets for the Elliott 803 and 503.

For the Elliott 803 and 503, two 19-bit instructions are packed into each 39-bit word. The pair of instructions is separated by a 'B-line' bit. When this bit is set, the second instruction is modified by adding to it the contents of the memory location specified by the address portion of the first instruction of the pair. (For the Elliott 503 only, the scheme was generalized by the 67 instruction – see later). This B-bit mechanism allows 'any' memory location to be used as an address-modifier (ie index register). There are no explicit hardware index registers within in the CPU.

The layout of a pair of instructions for the Elliott 803 and 503 is as follows:

6	13	1	6	13
F	N	B	F	N
Op. code	Address, constant or device	B indicator	Op. code	Address, constant or device

N can either be a memory address or a constant (literal) or an input/output device specifier, according to the function as specified by the Op.code bits. It is always a memory address for instructions in groups 0 to 4, as shown below. N is used as a constant (literal) for instructions 50, 51, 54, 55. It should be set to 4096 for instruction 65 and as an address in instructions 73 and 77. Its use for other input/output instructions is described later. On the computer's control panel there is an array of 39 hand-switches called the *word generator*. The number set up on these switches may be read into the accumulator via the 70 instruction. By convention, the op.code (function bits) for each instruction are written as two octal digits, thereby covering the range 00 to 77.

Arithmetic is normally single-length, two's complement, with fixed-point values being held in the range $-1 \le x < +1$. The single-length accumulator is extended by an auxiliary register AR for those instructions which involve double-length working. From the programmers' viewpoint, 39-bit floating-point numbers are held in the form:

$$x = a.2^b,$$

where: $-1 \le a < -\frac{1}{2}$ or $a = 0$ or $\frac{1}{2} \le a < 1$ and $-256 \le b < 256$.
Actually, the exponent is held internally as $(b + 256)$, so that $0 \le b < 255$, leading to a more-convenient representation of floating-point zero [6].

Instructions in groups 0 to 3 are symmetrical, the main difference between the groups being the sequence of implied memory operations at the detailed hardware level. The Elliott 803 and 503 have a magnetic core store with destructive-read properties. Thus a *read* must always be followed by a *write* operation. For group 0 instructions, it is the *old (former)* contents

n of the memory location that is written back. For group 1 it is the old contents of acc, a, that is written back. For groups 2 and 3, it is some function of {a,n} that is written back. This hardware symmetry means that many of the instructions in groups 1, 2 and 3 may seem curious to the modern programmer. To emphasise the point, only the mnemonics of instructions 00 to 37 that would now be regarded as standard practice are emboldened in the description below.

The instruction set(s) which follow come from the two Elliott booklets entitled *803 FACTS* and *503 FACTS* (references 14 and 15). The definition of instructions with Op. codes 00 to 65 is identical for the 803 and 503 computers. Instructions in the range 66 to 77 are concerned with input and output and their definitions differ between the 803 and the 503, as explained later. Actually, the special instructions 66 and 67 are simply described as *not used* in reference 14, because they were only enabled for Process Control applications of the Elliott 803 computer. Information on the 66 and 67 instructions for the 803 comes from references 10 and 11.

Notation. In defining the 00 to 37 instructions for the Elliott 803 and 503 computers, we employ the following notation. The 'old' and 'new' contents of memory location N are denoted by **n** and **n'** respectively. Similarly, the 'old' and 'new' contents of the accumulator are denoted by **a** and **a'**. For instructions in the range 50 – 77, the **N** bits are sometimes used as a constant (literal), sometimes as a memory address and sometimes as an extension of the F bits (thereby defining further sub-operations). When used to extend the F bits, N must be given one of a set of specific values, such as 4096, as indicated below. Finally, **AR** denotes the *Auxiliary Register,* used for example in double-length operations.

Op.code	***a'***	***n'***	***modern mnemonic and explanation***	
00	a	n	**NOP**	no operation
01	-a	n	**NEG**	negate accumulator
02	n +1	n	**LDINC**	load acc & inc.
03	a &n	n	**AND**	
04	a +n	n	**ADD**	
05	a -n	n	**SUB**	
06	0	n	**CLR**	clear acc
07	n -a	n	**REVSUB**	reverse subtract.
10	n	a	**SWAP**	swap acc & memory
11	-n	a	SWAPN	swap & negate
12	n +1	a	SWINC	swap & inc.
13	a &n	a	SWAND	swap & AND
14	a +n	a	SWADD	swap & ADD
15	a -n	a	SWSUB	swap & SUB
16	0	a	STCLR	store & clear
17	n -a	a	SWRSUB	swap & rev. SUB.
20	a	a	**STO**	store acc
21	a	-a	**STN**	store acc negatively
22	a	n +1	**INCM**	increment memory
23	a	a &n	STAND	store & AND memory
24	a	a +n	STADD	store & ADD
25	a	a -n	STSUB	store & SUB

26		a	0	**CLM**	clear memory
27		a	n -a	STRSUB	store & rev. SUB.
30		n	n	**LDA**	load acc
31		n	-n	LDMNEG	load acc & negate memory
32		n	n +1	LDMINC	load acc & inc. memory
33		n	a &n	LDMAND	load acc & AND into memory
34		n	a +n	LDMADD	load acc & ADD into memory
35		n	a -n	LDMSUB	load acc & SUB into memory
36		n	0	LDMCLR	load acc & clear memory
37		n	n -a	LDMRSUB	load acc & rev. SUB into memory.
40,	44			JMP	unconditional jump
41,	45			JNEG	jump if acc negative
42,	46			JEQ	jump if acc equals zero
43,	47			JOV	jump if fxpt overflow, & reset overflow indicator.

(40 to 43 transfer to the first instruction of a pair starting at address N; 44 to 47 transfer to the second instruction of a pair).

50			SHRD	arith. shift of the double-length acc right by N places.
51			SHRS	shift acc logically right N times; clear AR.
52	a xn	n	MPYD	multiply acc by n, giving a double-length product.
53			MPYS	single-length multiply by n; clear AR.
54			SHLD	shift the double-length acc left by N places.
55			SHLS	shift acc left N times; clear AR.
56	a /n	n	DIV	divide (double-length dividend, single-length quotient). Clear AR.
57			LAR	read AR to acc.
60	a +n	n	FLADD	floating-point add; clear AR.
61	a -n	n	FLSUB	floating-point subtract; clear AR
62	n -a	n	FLRSUB	floating-point reverse-subtract; clear AR
63	a xn	n	FLMPY	floating-point multiply; clear AR
64	a /n	n	FLDIV	floating-point divide; clear AR
65		4096	CONFL	convert the integer in acc to a normalised Floating point number; clear AR
65		0 -> 39	SHLC	shift acc circular (end-around) upwards N places.
70			HKY	read the control-panel handkeys *(word generator)* into the accumulator.
73			SETLNK	write the address of the present instruction to memory location N. *(Used for subroutine return).*

The action of all of the foregoing instructions is identical for the Elliott 803 and 503 computers. The rest of the instructions are defined differently for each machine, as now explained.

Instructions in the range 66 – 77 for the Elliott 803.

66	a/n	n	DIVSH	divide acc by operand, placing 13-digit quotient in

		acc. *(NB – only for Process Control applications).*
67	SQRT	extract square root of acc, placing 13-digit root in acc. *(NB – only for Process Control applications).*

The rest of the Group 7 instructions are specific to the Elliott 803's input/output devices, so have been arranged below accordingly. As Laurie Bental (formerly of Borehamwood) remarked, "The beauty of the Group 7 input/output instructions is that the set is extremely flexible. In general the instruction specifies the function and the address of the device. 72 and 73 were extensively used for process control where there are a large number of transducers etc. 76 and 77 were used for a variety of block transfer devices many of which were not even envisaged when the [803] processor was designed".

(a) 803 Instructions for paper tape reader, punch and teleprinter:

71	0	read a char. from the first tape reader to accumulator.
71	2048	read a char. from the second tape reader to accumulator.
74	N	punch the char. N on the first tape punch.
74	2048 + N	punch the char. N on the second tape punch
74	4096 + N	print the char. N on the teleprinter.

(Paper tape reader, punch and teleprinter channels include *busy* line facilities).

Instructions 75, 76 and 77 were used for a variety of input/output devices, as described later from the programmers' viewpoint. First, though, a general engineering description of these instructions is given. The engineering account is taken from reference 16.

(b) Engineering description of 803 instructions 75, 76 and 77.

75 Input or output the 13 least-significant digits to or from the Accumulator. Device and function are specified by the N bits. (In the case of input, the Acc is first cleared). Time taken: two word-times.

76 Output 13 bit Address code and 40 bit store code. (Prepare to input or output into or out of store. Device and function specified by code). Also clear Acc and input control word into 13 l.s.digits of Acc. Time taken: three word-times.

77 Block transfer from peripheral device into or out of store, starting at address specified. Every 77 instruction must be preceded by a 76 instruction. Timing of block transfer is under peripheral control. The Elliott 803's maximum transfer rate of information is one 39-bit word every 144 microseconds.

Now follows the programmers' descriptions, as given in the 803 FACTS booklet (reference 14).

(c) 80-column punched card input and output for the Elliott 803:

76	512	read card input control word; prepare to read card.
77	N	read card to store locations N to N + 79.
76	2561	read card output control word; prepare to punch a card.
77	N	punch the information held in store locations N to N + 79. (Actual punching takes 600 milliseconds per card).

(d) Magnetic film store instructions for the Elliott 803:

75	1027 read address of last block read or written.
76	1024, 1032, 1040 or 1048: read handler control word to accumulator; prepare to read on film handler 1, 2, 3 or 4.
76	1025, 1033, 1041 or 1049: read handler control word to accumulator; prepare to

write on handler 1, 2, 3 or 4.

76 1026, 1034, 1042, 1050: read handler control word to accumulator; prepare to search on handler 1, 2, 3 or 4.

77 N read, write or search as prescribed by a 76 instruction.

(e) Digital plotter instructions for the Elliott 803:

72 7169, 7170, 7172, 7176: pen moves in direction E, W, N, S.

72 7173, 7174, 7177, 7178: pen moves in direction NE, NW, SE, SW.

72 7184, 7200: pen raise, or pen lower.

(f) Anelex Lineprinter instructions for the Elliott 803:

76 3073 read Anelex control word to accumulator; prepare to print one line.

77 N transfer to lineprinter from store locations N to N + 120. The contents, M, of location N controls the lineprinter's paper-feed as follows:

$M \leq 0 \leq 30$	feed M + 1 lines and print.
M = 31 or 32	print on the same line.
$M \leq 33 \leq 62$	find channel M and print.
M = 63	find top of form and print.

Instructions in the range 66 – 77 for the Elliott 503.

The 66 and 67 instrructions, which are used for special process control purposes in the 803, are re-defined as follows for the 503:

66	SWITCH	load registers and transfer control. Used for returning from Interrupt. Time taken: 19.5 microseconds.
67	MOD	modify the next instruction by adding to it the least-significant 19 digits of n. Time taken: 7.2 microsecs.

The 503 incorporates a fully autonomous facility for controlling the transfer of data between its CPU and its peripheral equipment, via 15 Autonomous Data Transfer (ADT) channels. Provision is made for autonomous transfers from more than one device to take place concurrently. Transfer rates can vary enormously, according to concurrent activity, with a maximum possible rate of about 100,000 words per second (reference 17). In addition to the usual input/output devices such as paper tape readers/punches, card readers/punches, lineprinters and digital incremental plotters, the Elliott 503's ferrite core backing store is also classed as a peripheral device. Autonomous transfers are used for moving blocks of data between the backing store and the primary store. Alternatively, single words may be transferred between the accumulator and the backing store.

For input/output instructions in group 7 orders, the N bits have the following format:

4	9
Device number	Special mode or control bits.

The 15 classes of peripheral device are allocated a fixed priority order. Of the nine special mode bits, the least three significant bits usually specify the operation to be performed whilst the remaining six bits specify the part of the peripheral to which the instruction refers if there is more than one part.

71	N	INCH	send N to Peripheral Controller. Input a 7-bit character from device N to acc
72	N	OUTW	send n to Peripheral Controller. Output a word from acc to device N.
74	N	SELN	send N to Peripheral Controller, for selection purposes and for information.
75	N	INWD	send n to Peripheral Controller. Input a Control Word from device N to acc
76	N	PREPAT	send N to Peripheral Controller. Prepare for an autonomous transfer to/from device N by reading a Control Word from device into acc.
77	N	EXAT	Execute the autonomous transfer previously set up via the 76 order, to/from memory location N. The CPU places protective tags on the area of memory involved in the transfer. The most significant part of the accumulator specifies the number of words, M, to be transferred.